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AN EFFICIENT, BROAD-BAND, SWITCHING-MODE AMPLIFIER WITH ISOLATED OUTPUT

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FOREWORD

This is a technical report of a study conducted by the Electrical Engineering Department, Auburn University, toward fulfillment of Contract NAS8-11344. This report represents a summary of the research conducted to date on the design of the output stages of a PWM amplifier with an isolated output.

AN EFFICIENT, BROAD-BAND, SWITCHING-MODE AMPLIFIER WITH ISOLATED OUTPUT

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ABSTRACT

This study is concerned with the design and development of the output power amplifier stage for a pulse-width-modulated amplifier with a frequency response from dc to 20 kHz. Dc isolation from the load is provided through the use of a ferrite-cored switching-transformer to transfer energy from the power amplifier to the load. The amplifier uses two channels, thus providing amplification for signals of both polarities. This scheme requires the use of output gating.

The amplifier uses a 200 kHz switching frequency which allows for the use of physically small components and gives the amplifier a broad-band response.

A bread-board model of the amplifier was constructed and tested. The amplifier exhibited a frequency response that is flat to within 0.5 dB from bipolar dc to 20 kHz. The dc efficiency is approximately 80% for both channels at power output levels of 1 to 2 watts. The results of all performance tests are presented graphically.

A design example for an amplifier which has an output of 7 volts rms into a 70-ohm load is presented. This amplifier is designed

using the design equations developed and presented in this report. The bread-board amplifier used for the performance tests is the same as the amplifier in the design example.

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I. INTRODUCTION

Switching-mode amplifiers are particularly useful whenever operating efficiency is of primary concern. They operate efficiently because the power handling transistors assume only two states -- "on" (saturation) and "off" (cutoff). When a transistor is "on" it is in a very low dissipation mode and when it is "off" it has zero dissipation. Transistor dissipation is higher during the transitions between saturation and cutoff, therefore faster turn-on and turn-off speeds increase the operating efficiency.

A pulse-modulated amplifier performs four basic functions: (1) The input signal is sampled; (2) each sample is used to modulate one of a train of pulses; (3) the pulses are amplified; (4) and finally the amplified pulses are demodulated to reproduce the input signal. The pulse-modulation can take the form of pulse-amplitude modulation (PAM), pulse-width modulation (PWM), or pulse-position modulation (PPM). This amplifier uses a PWM scheme which keeps all transistors "off" in the absence of an input signal, thereby reducing quiescent losses virtually to zero. This is analogous to class-B operation of conventional amplifiers.

The PWM amplifier developed has a frequency response from dc to the neighborhood of one-tenth the switching-frequency. A high switching-frequency not only increases the pass-band but also permits the use of

smaller components, such as the output transformer and the output filter.

The circuitry required in a PWM amplifier is more complex than that used in conventional class-A or class-B amplifiers. A considerable amount of signal distortion and carrier intermodulation noise is introduced which is removed through the use of an output filter and negative feedback. High speed transistors, that must carry relatively high currents are required.

The block diagram of a complete PWM amplifier is shown in Figure 1-1. This study is concerned with the design of the output stages, therefore the input amplifier and sawtooth generator design were not considered. A PWM signal from a PWM signal generator[1] is fed directly into the crossover detectors.

Figure 1-2 illustrates some typical wave-forms for the indicated test points on the block diagram. Waveforms within the output stage itself are omitted here but are explained in detail in Chapter III.

The typical PWM waveforms in Figure 1-2 are described in a previous study.[2] The switching-frequency to signal-frequency ratio utilized is much higher than that depicted in the figure.

The schematic diagram of the crossover detectors, drivers, output amplifiers, and output filter is shown in Figure 1-3. Each of these sections is treated separately. The P and N channels complement each other therefore it is necessary to consider only one channel throughout. The operation of the P channel is presented in the ensuing chapters.

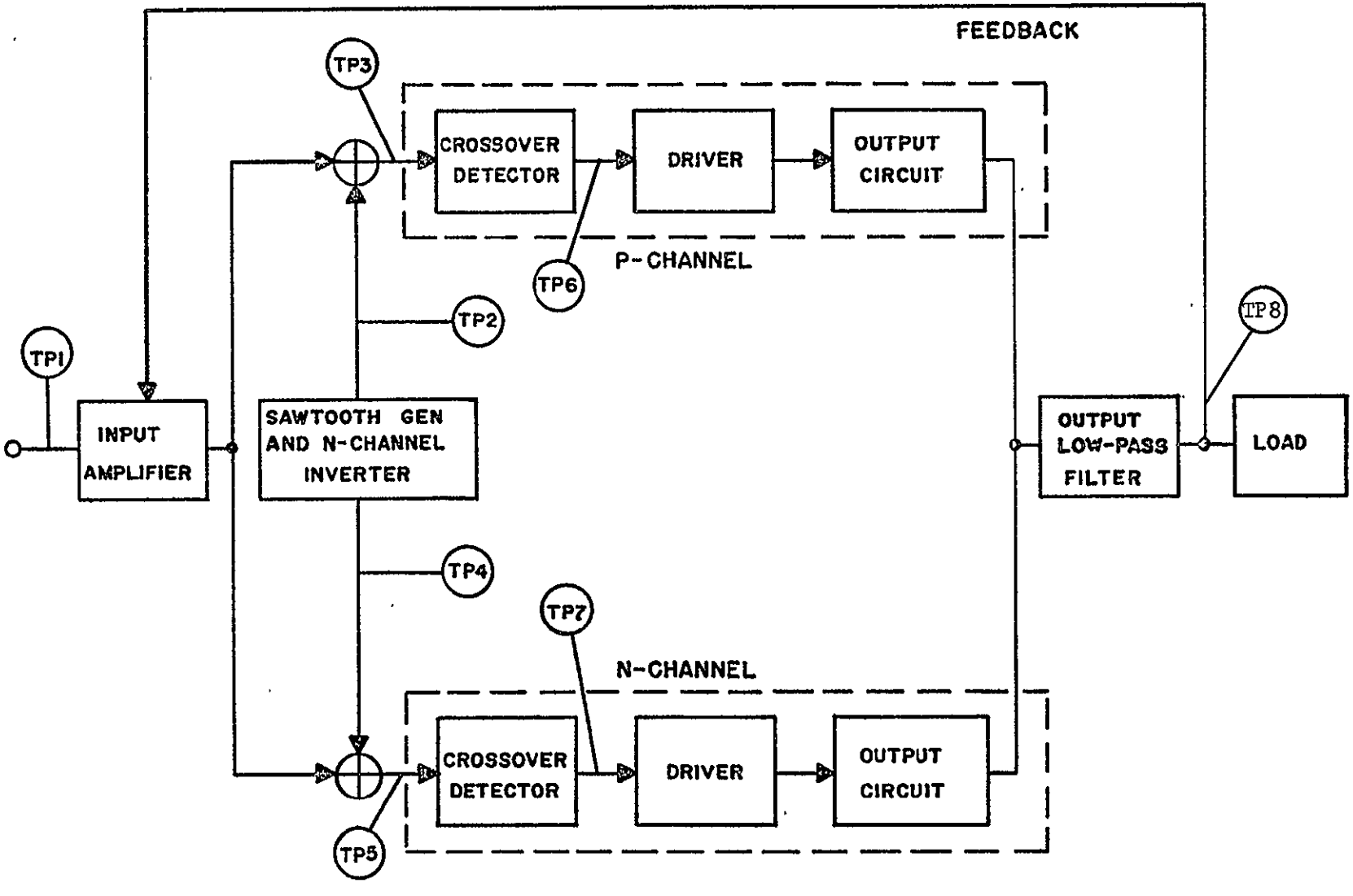
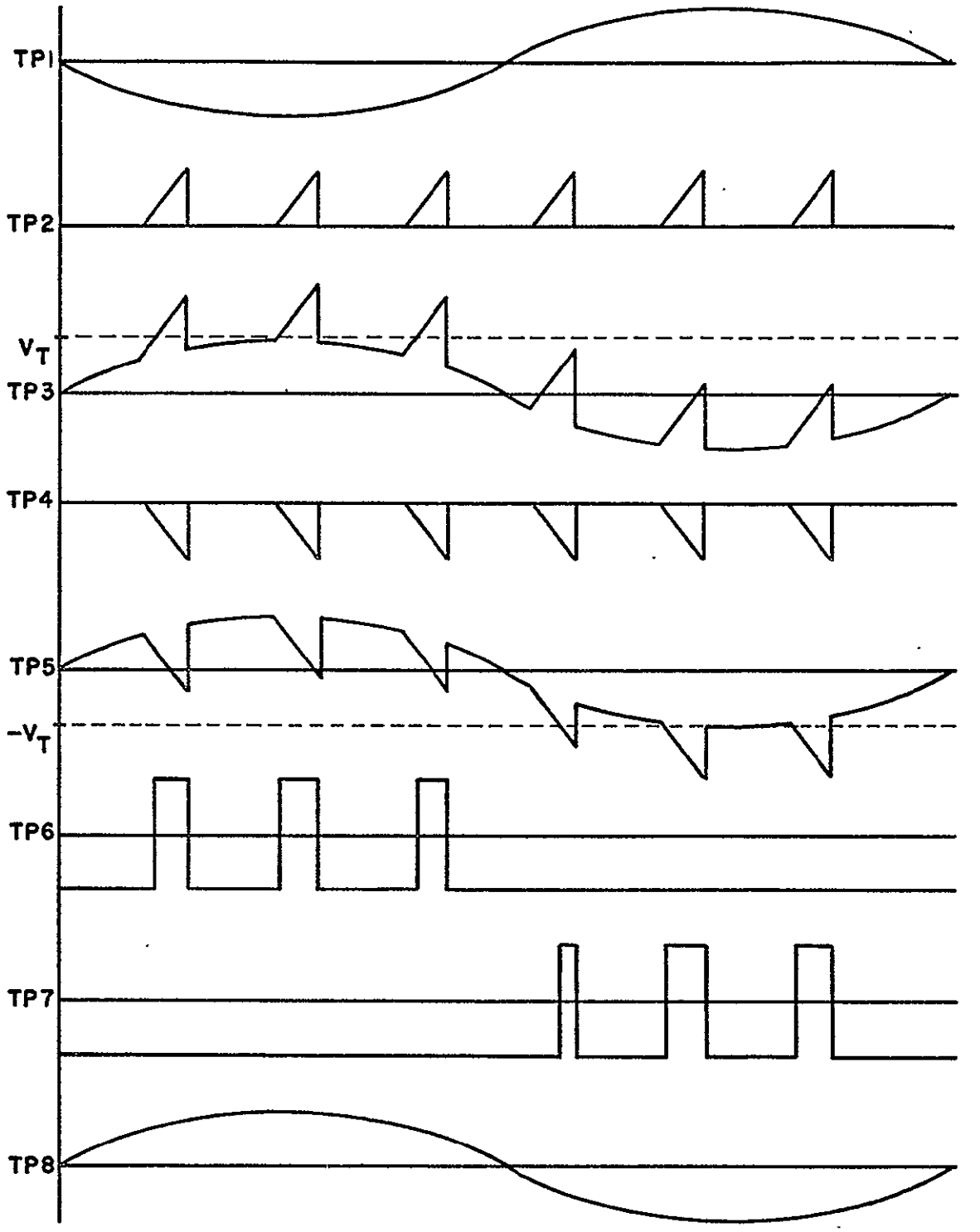


Figure 1-1. Block diagram of PWM amplifier.



V_T = P-CHANNEL CROSSOVER DETECTOR THRESHOLD
$-V_T$ = N-CHANNEL CROSSOVER DETECTOR THRESHOLD

Figure 1-2. Test-point waveforms for Figure 1-1.

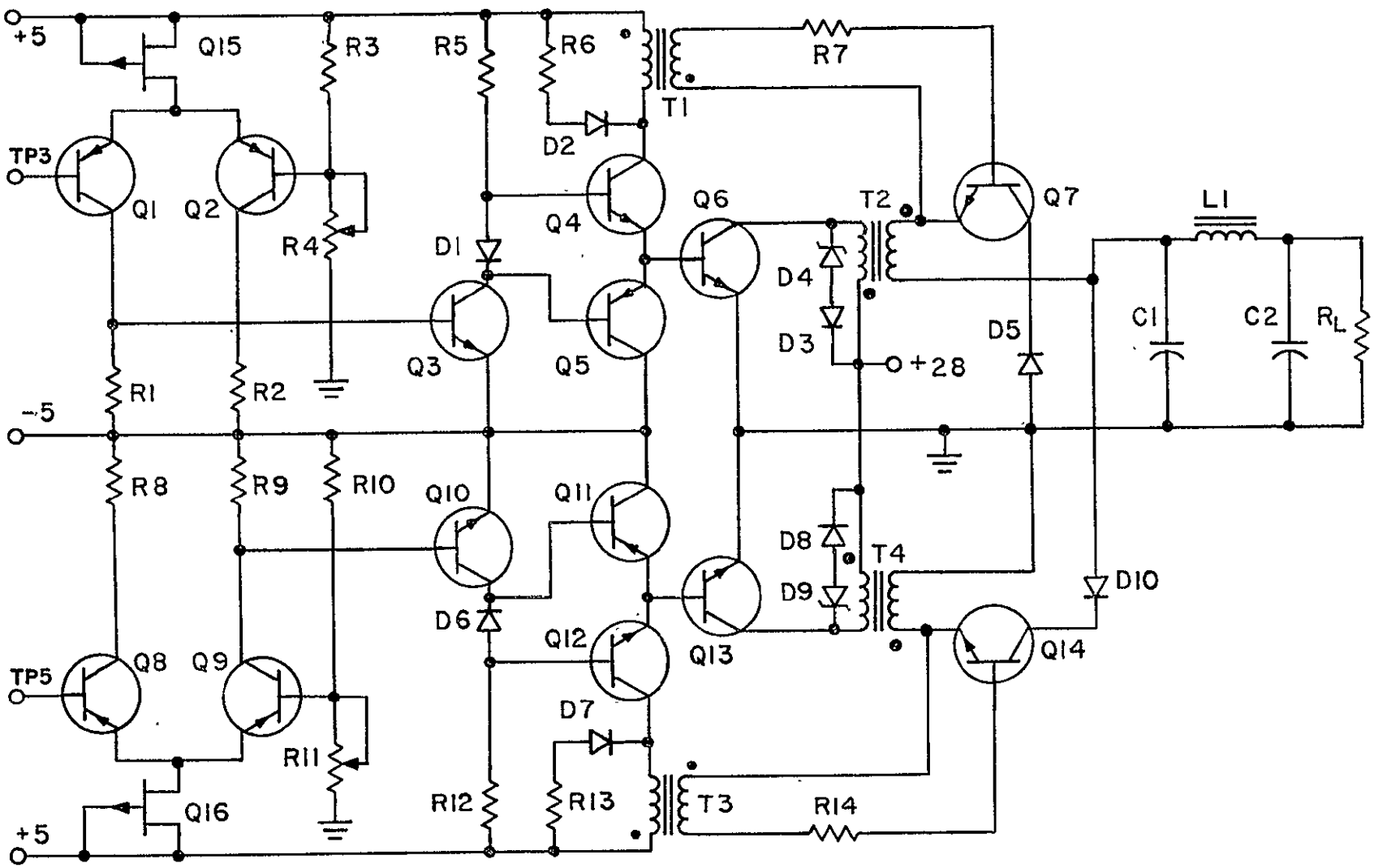


Figure 1-3. Schematic diagram of detectors, drivers, and output stage.

II. CROSSOVER DETECTOR AND WAVESHAPER

The crossover detector distinguishes whether its input signal is above or below a certain threshold level, and derives its output accordingly. This detector consists essentially of a differential amplifier with a constant-current source in the emitter. Figure 2-1 shows the schematic of the P-channel crossover detector.

A field-effect transistor (FET) with the gate and source tied together provides a constant-current source of 5 ma. The voltage divider of R3 and R4 biases Q2 "off" with a positive voltage, V_T, which is set at the desired threshold value. The N-channel detector uses a threshold of $-V_T$ on Q2 and takes its output from Q2 rather than Q1. The total signal information is thus retained in the positive pulses of the P or of the N channel. The circuitry for the remainder of this section is identical for both channels. Since Q2 is normally "off", the current source assures that Q1 is normally "on". Under these (static) conditions, R1 has a voltage drop across it which is clamped to approximately 0.5 V by a base-emitter junction in the next stage. This will put e_1 at -4.5 V. When the signal voltage e_s is greater than the threshold voltage V_T, Q1 turns "off" and Q2 conducts. The signal e1 drops to -5 V. When es drops below V_T, then Q1 again conducts, returning e_1 to -4.5 V. The signal, e_1, is fed to the waveshaper, which is shown in Figure 2-2.

When the input signal is -4.5 V the base-emitter junction of Q3

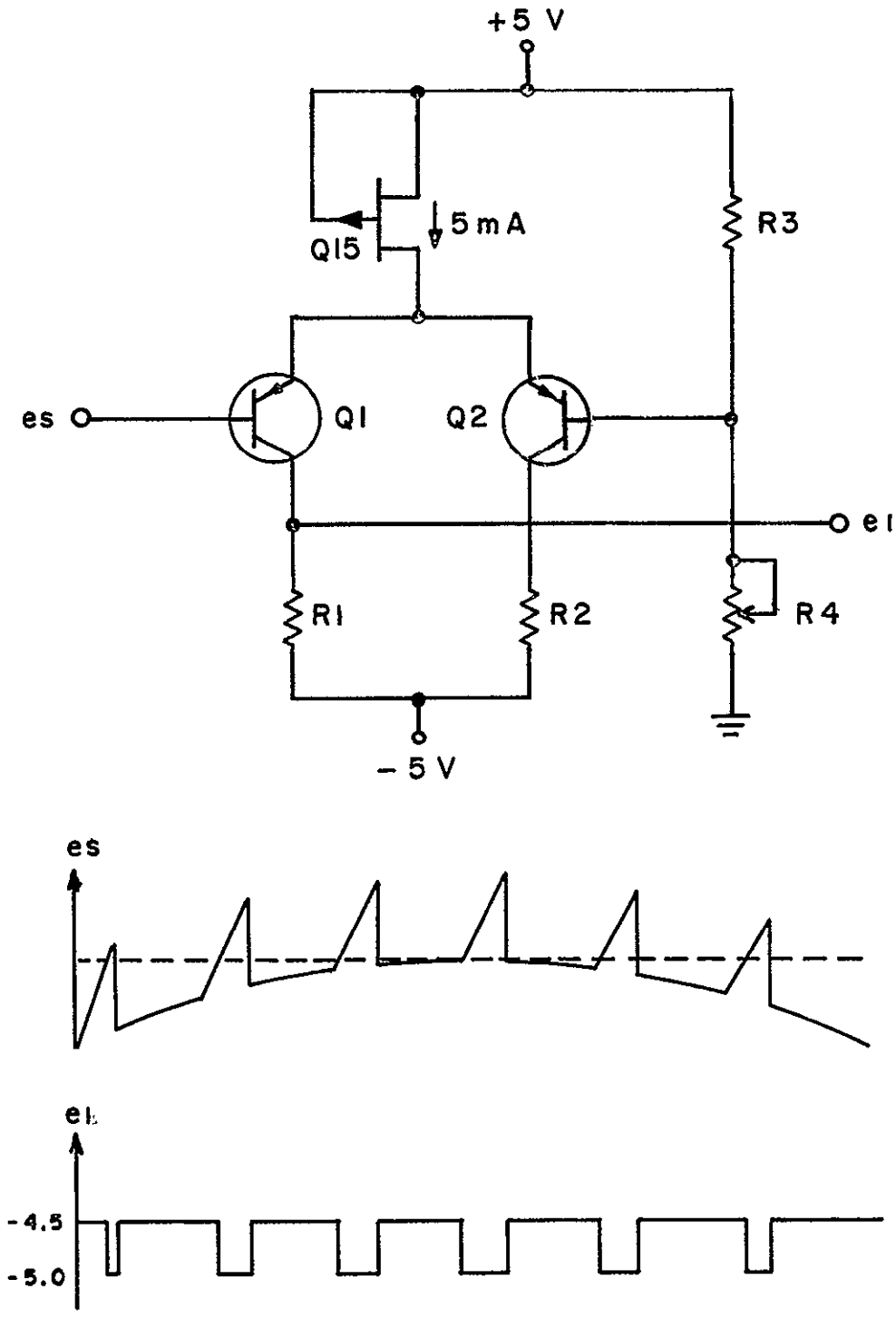


Figure 2-1. P-channel crossover detector and associated waveforms.

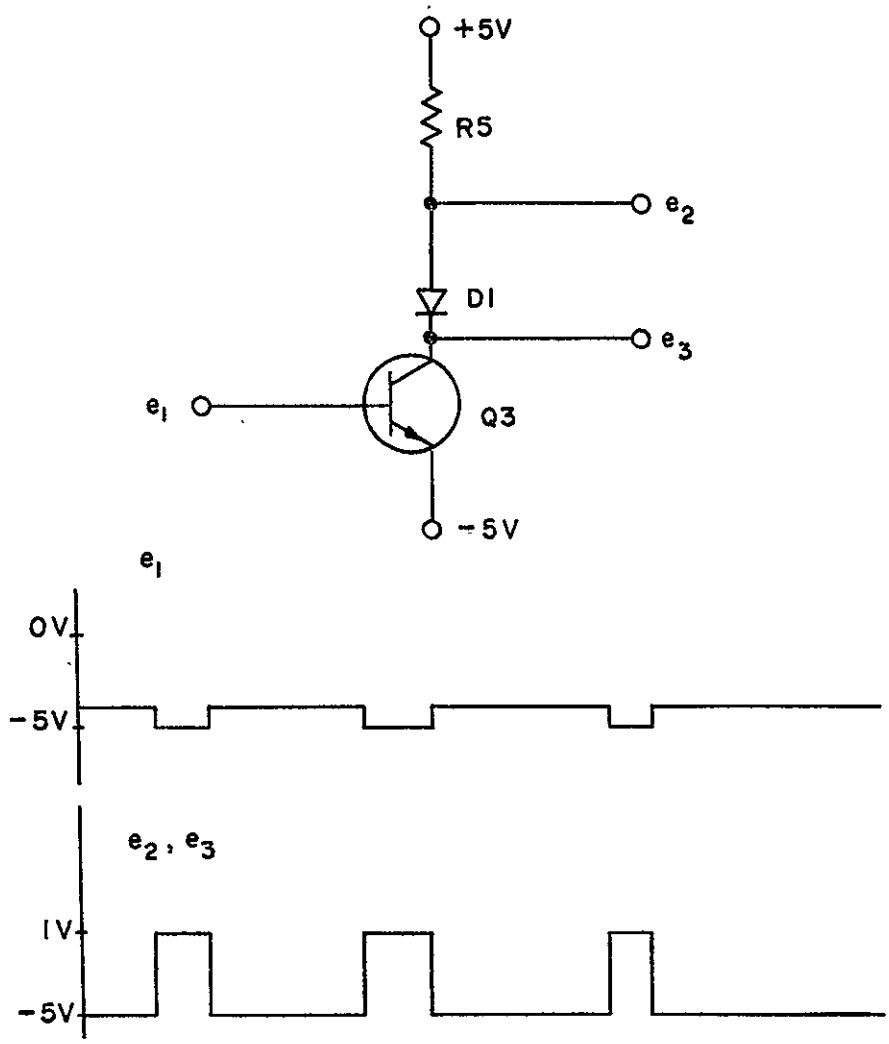


Figure 2-2. Schematic diagram of waveshaper.

is forward biased and conducts. It is desirable for the waveshaper to provide as much drive as possible to the next stage, therefore Q3 must have sufficient drive to saturate. The equivalent circuit of the collector-current path is shown in Figure 2-3(a). It can be seen from the diagram that:

$$I = \frac{5V - e_2}{R5} . \tag{2.1}$$

two forward-biased transistors placed in series clamp e_2 to approximately 1.0 V, therefore (2.1) yields:

$$I = 4 \text{ mA}.$$

Figure 2-3(a) also illustrates

$$I_C = I - I_D \tag{2.2}$$

I_o drives an NPN transistor and must be positive, therefore:

$$I_C < I = 4 \text{ mA}.$$

The transistor used for Q3 can be saturated with a base current of $I_B = 0.2$ mA under these conditions. Figure 2-3(b) illustrates that $(I_1)\ (R1) = V_{BE}$. If V_{BE} is estimated to be 0.5 V, which is typical of silicon transistors, then

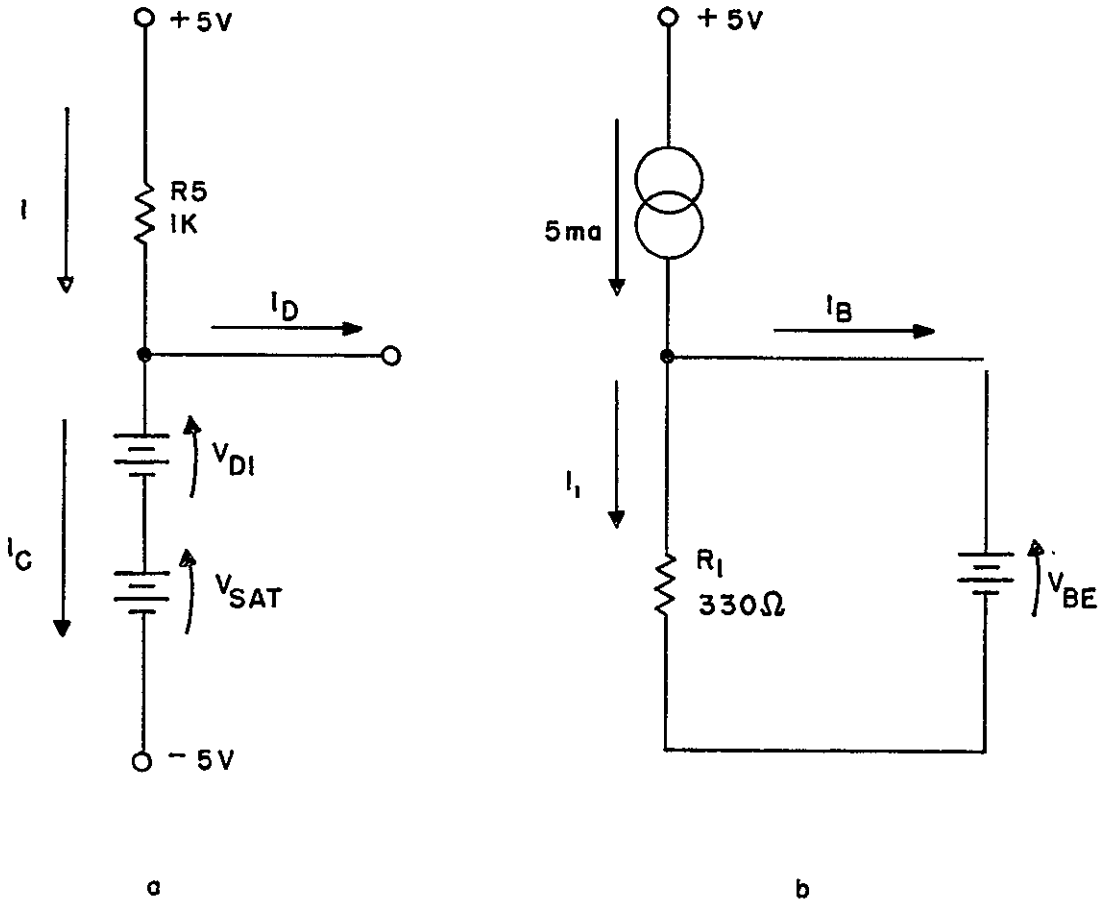


Figure 2-3 (a) Equivalent circuit of collector current path of Q3.

(b) Equivalent circuit of base current path of Q3.

$$I_1 = \frac{0.5 \text{ V}}{R1} = 1.5 \text{ mA}. \tag{2.3}$$

Likewise;

$$I_B = 5 \text{ mA} - 1.5 \text{ mA} = 3.5 \text{ mA} \tag{2.4}$$

which is more than sufficient to saturate Q3. When Q3 is "on" both e_2 and e_3 are approximately -5.0 V. When e_1 goes to -5.0 V Q3 is biased "off". Thus e_2 and e_3 are clamped to approximately 1.0 V. The diode (D1) serves to reduce the delay times of the transistors driven by e_2 and e_3.

III. DRIVER AND OUTPUT AMPLIFIER

The function of the driver amplifier is, as its name implies, to provide sufficient current to saturate the output amplifier. Switching speeds are critical at this point since the currents being switched are large. With the increased current, undesirable transistor dissipation also increases. The actual transition time is reduced by using a large overdrive factor.[3]

The schemetic diagram for the P-channel driver and output stages are shown in Figure 3-1. The driver amplifier alone is shown in Figure 3-2. The input to the driver amplifier is obtained from the waveshaper, which was covered in Chapter II.

Whenever e_2 and e_3 are at -5 V, Q5 is "on" and e_4 is held at approximately -4.5 V, cutting "off" Q6. Care is taken not to exceed the reverse bias breakdown voltage of Q6.

When e_2 and e_3 go positive Q4 is driven to saturation. The emitter current of Q4 is the base drive for the power amplifier Q6. It is desirable for Q6 to saturate as soon as possible after Q4 turns "on".

Energy obtained from the collector current of Q4 is used to open the output gate and is coupled there by way of T1. Figure 3-3 illustrates some possible drive-current waveforms. If the primary winding of T1 (L_{Pn}) were the only load for Q4 the drive current would take the form of a ramp such as I_{D1} in Figure 3-3. However, if I_Q represents

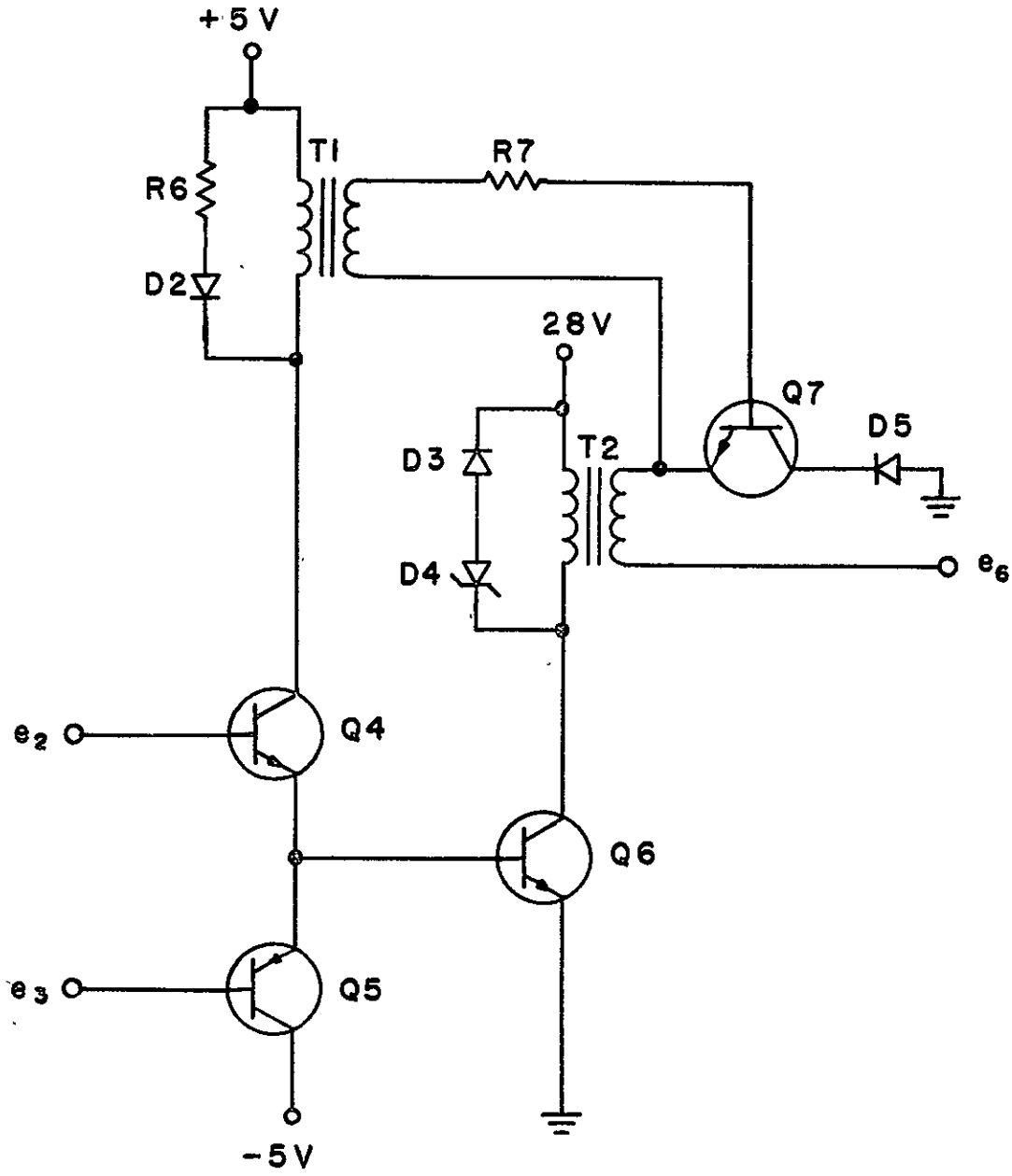


Figure 3-1. Driver and output stage

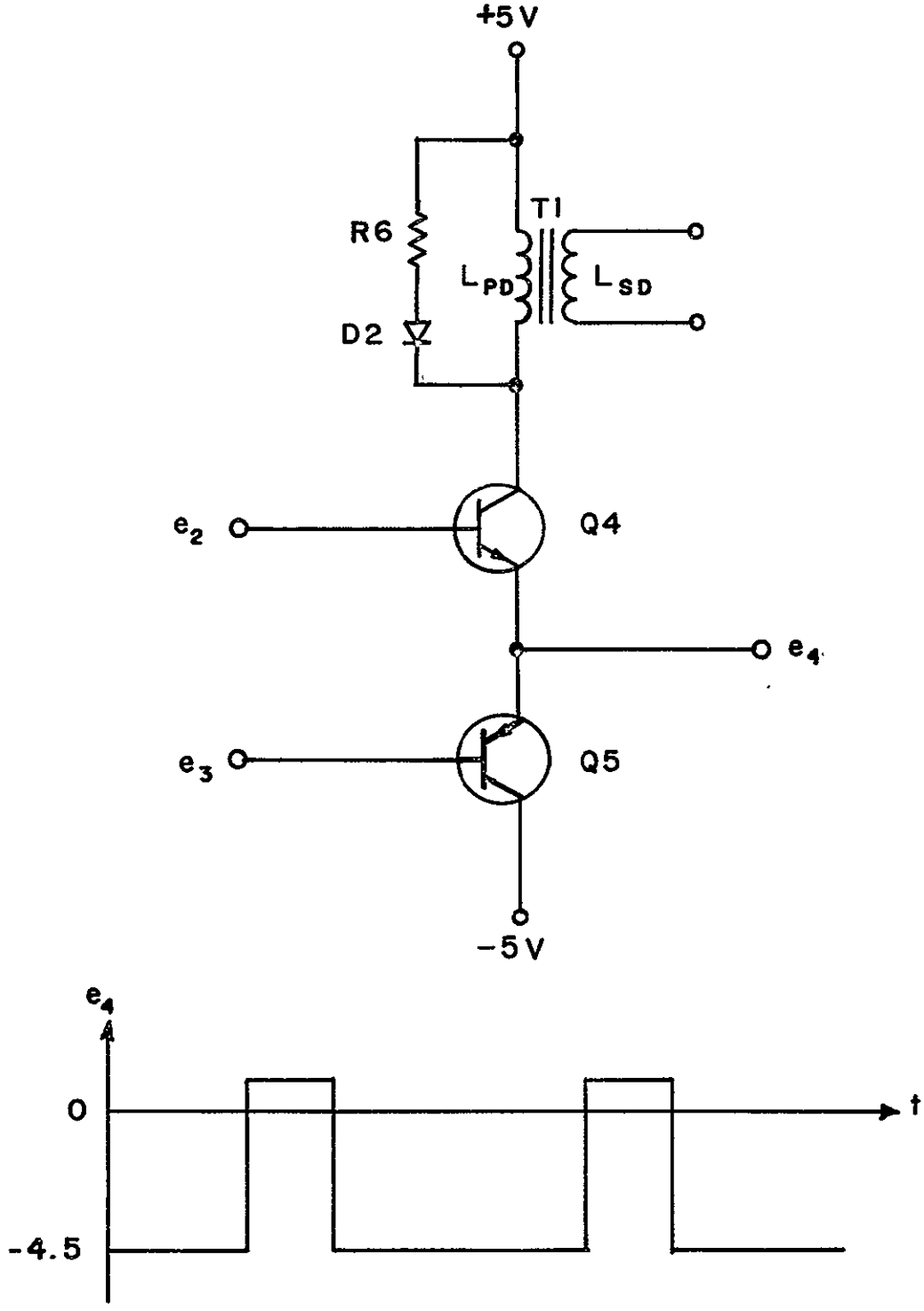


Figure 3-2. Driver amplifier and output waveform.

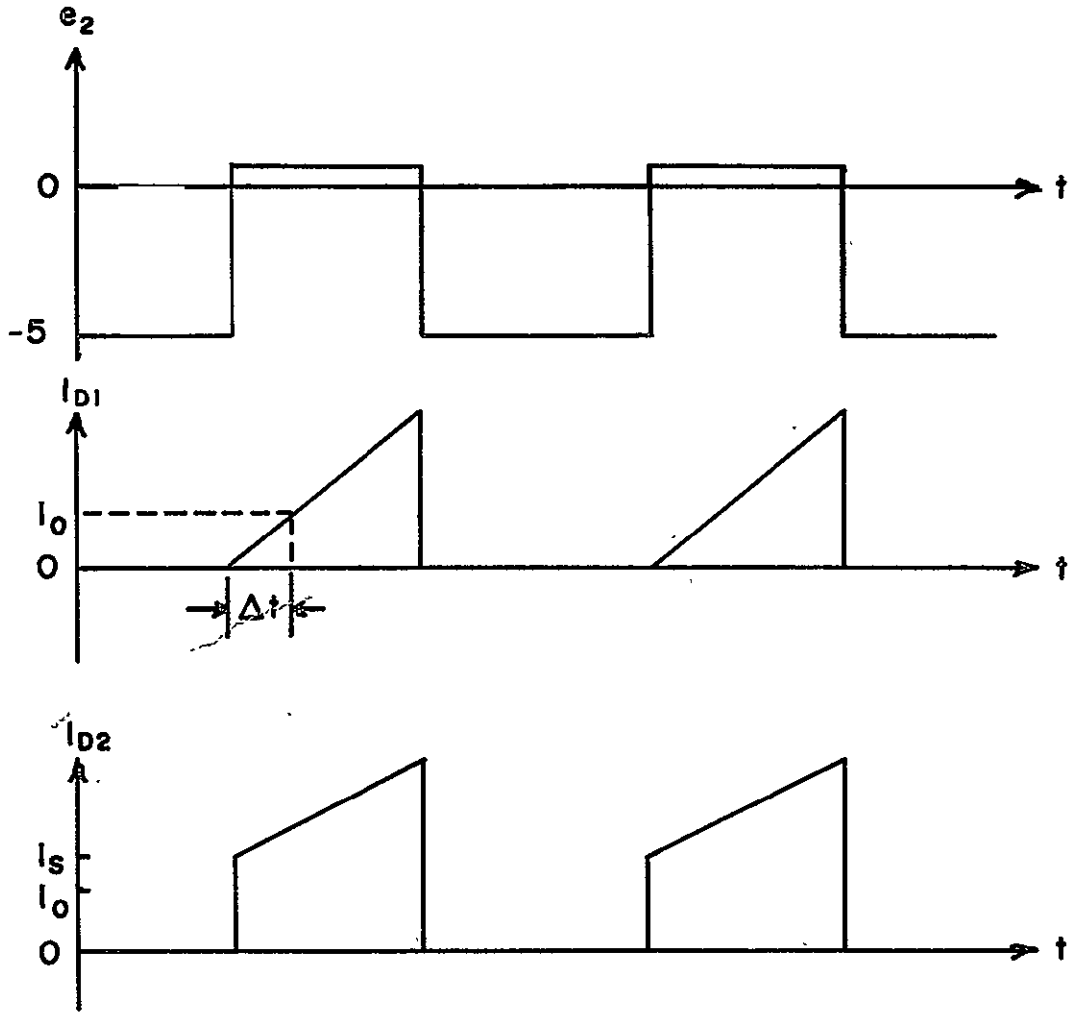


Figure 3-3. Drive current waveforms.

the minimum current required to saturate Q6 then the output pulse would be effectively Δt seconds shorter than the input pulse. This causes an undesirable slow turn "on" of Q6. Resistor R6 is shunted across L_{PD} and an initial start current (I_S) is provided for the base drive of Q6 (see I_{D2} in Figure 3-3). The only requirement to be met is that $I_S > I_O$. This enables Q6 to turn "on" at the prescribed time. The use of a diode (D2) in series with R6 is necessary so that R6 will not load the transformer when Q4 is "off". Further analysis of the gate drive is considered later.

The power amplifier is shown in Figure 3-4. The collector current of Q6 is a ramp. With this output it is obvious that switching speeds are much more crucial when turning Q6 "off". A quick turn "off" is accomplished here by the operation of Q5 (see Figure 3-2). As Q4 turns "off", the drive current is removed and Q6 begins turning "off". At the same time, Q5 is turned "on" thereby draining the base of Q6 of excessive base charge that has accumulated, forcing it to the "off" condition rapidly.

The power amplifier is "on" for a period of time T_{ON} (see Figure 3-4), which is approximately equal to the width of the base pulse. The saturation voltage of Q6 (V_{SAT}) increases, slightly, as the collector current increases, due to the saturation resistance of the transistor. When Q6 turns "off" e_5 returns to a potential equal to the 28-V supply plus the output voltage, V_O, which is reflected back across T2. T2 is used as a switching transformer and considerations concerning its operation and construction are taken up in Appendix A.

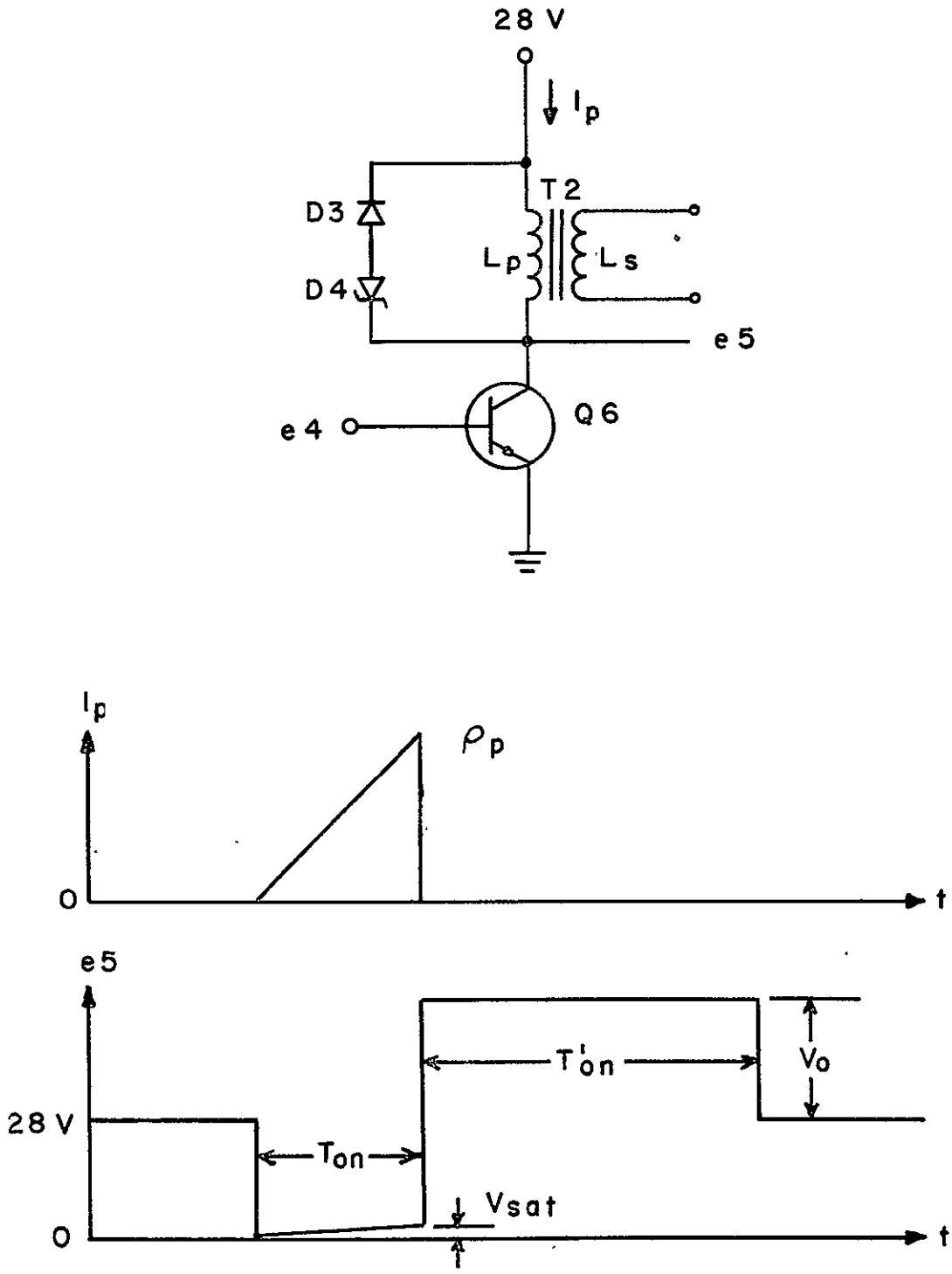


Figure 3-4. Power amplifier and associated waveforms.

The switching transformer is operated in such a manner that the field is time-shared by the primary and secondary. When current flows in the primary winding, the secondary circuit is an open circuit. The primary current builds up a field during its "on" time. When the primary is "off" and the secondary is "on", no current is allowed to flow in the primary. When the field collapses, all the energy is transferred to the secondary.

The waveform of e_5 shown in Figure 3-4 is an idealization. The typical waveform is illustrated in Figure 3-5(a). The voltage spike which occurs when Q6 is cut "off" is caused by small, unavoidable, leakage inductance in the transformer. This voltage spike may exceed the break-down voltage of Q6 and must be limited to a safe value. The diode, D3 (see Figure 3-4), would eliminate the spike entirely but would also short out the output voltage (V_0). The Zener diode, D4, allows e_5 to reach a voltage of V_Z above the supply voltage where $V_Z > V_0$. The response of the series combination of D3 and D4 is shown in Figure 3-6. The actual output voltage is shown in Figure 3-5(b) along with the base voltage of Q6. When Q6 is "on" the equivalent circuit of the power amplifier reduces to that of Figure 3-7. $I_p(t)$ is found by writing the differential equation:

$$L_P \frac{dI_P}{dt} + V_{SAT} - 28\ V = 0 \qquad (3.1)$$

with initial condition, $I_p(0) = 0$. V_{SAT} is the saturation voltage of Q6, and is negligible compared to the supply voltage. Neglecting V_{SAT}

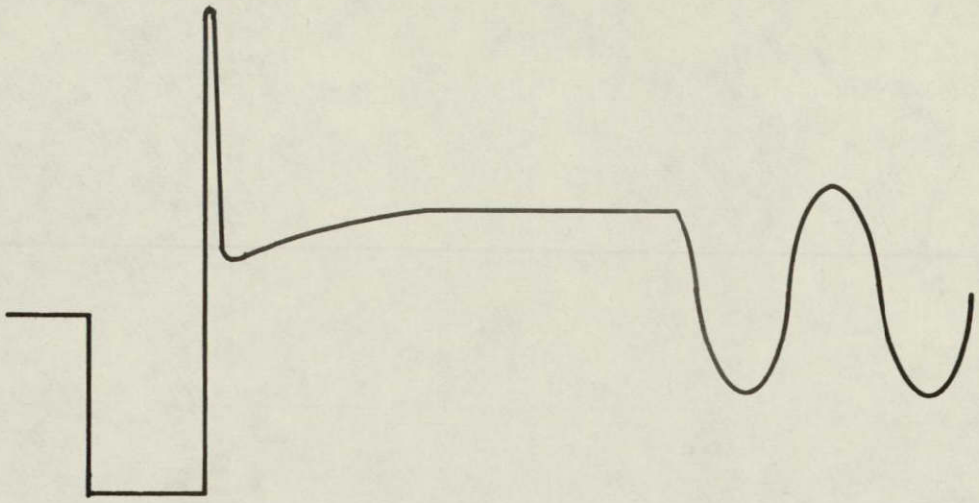


Figure 3-5 (a). Voltage waveform at collector of Q6.

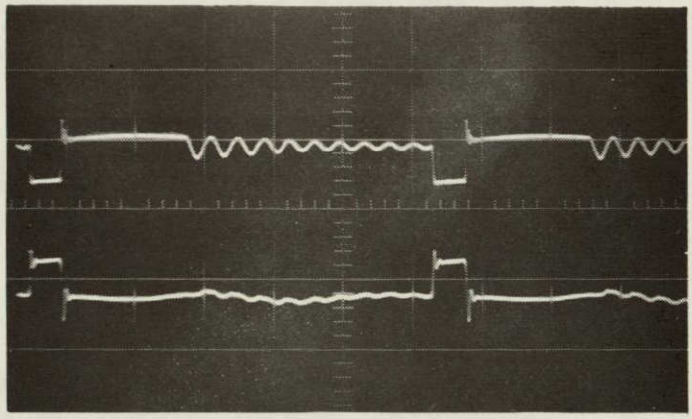


Figure 3-5 (b). Upper trace - Voltage waveform at collector of Q6.
Lower trace - Voltage waveform at base of Q6.

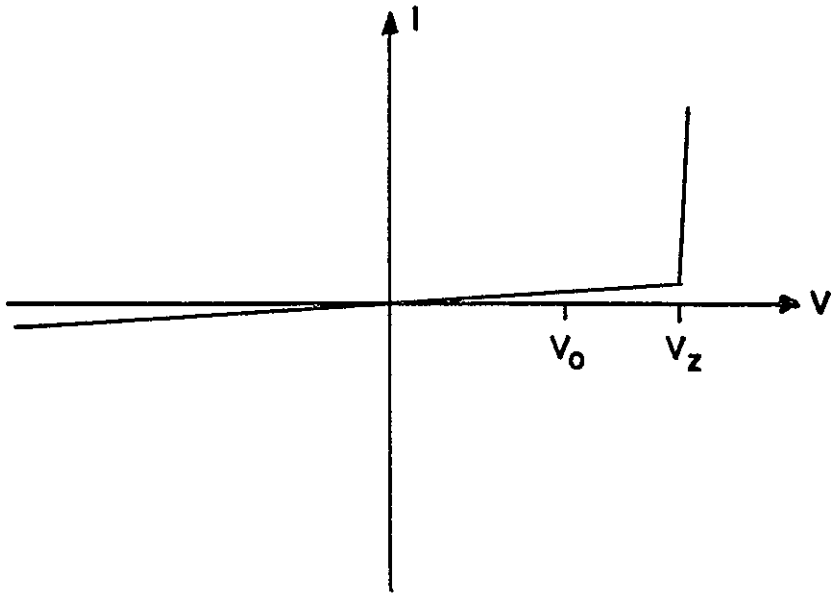


Figure 3-6. Response of D3 and D4.

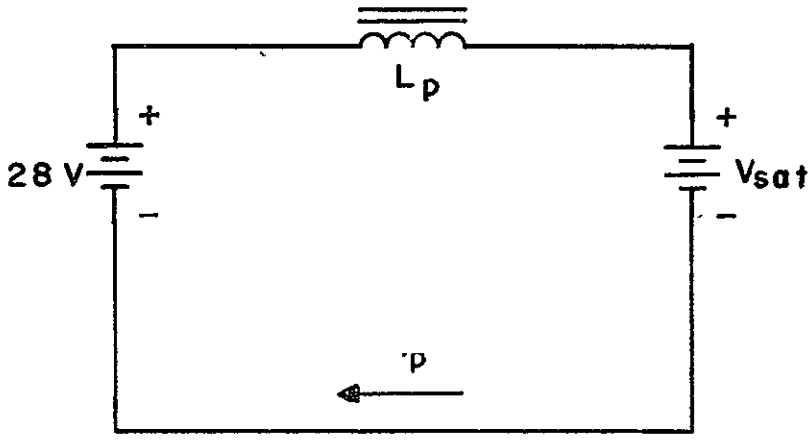


Figure 3-7. Equivalent circuit of the power amplifier when Q6 is "on".

and taking the Laplace transform of equation (3.1) yields:

$$sL_P I_P(s) = \frac{28}{s} \tag{3.2}$$

or

$$I_P(s) = \frac{28}{L_P S^2}$$

Thus

$$I_P(t) = \frac{28}{L_P} t \tag{3.3}$$

which is a ramp with a maximum value at $t = T_{ON}$, if ρ_P is the primary current at the instant Q6 is cut "off" (i.e. $\rho_P = \frac{28}{L_P} T_{ON}$). Figure 3-8(a) shows the secondary circuit of the output stage. The initial current in the secondary winding, L_S, is:

$$\rho_S = \rho_P \frac{N_P}{N_S} \tag{3.4}$$

At this same initial time, the gate transistor Q7 is saturated and the equivalent circuit of this stage is reduced to that of Figure 3-9. V_{OUT} is the load voltage and can be considered constant throughout the switching period because of a large input capacitor to the filter. The differential equation for the circuit is:

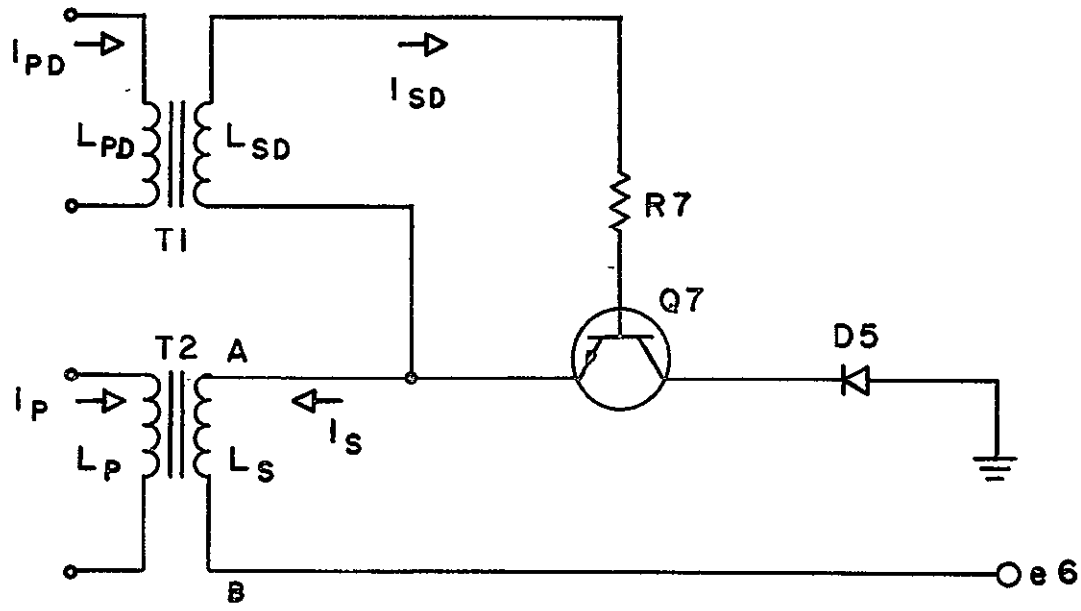


Figure 3-8 (a). Schematic diagram of output transformer and gate.

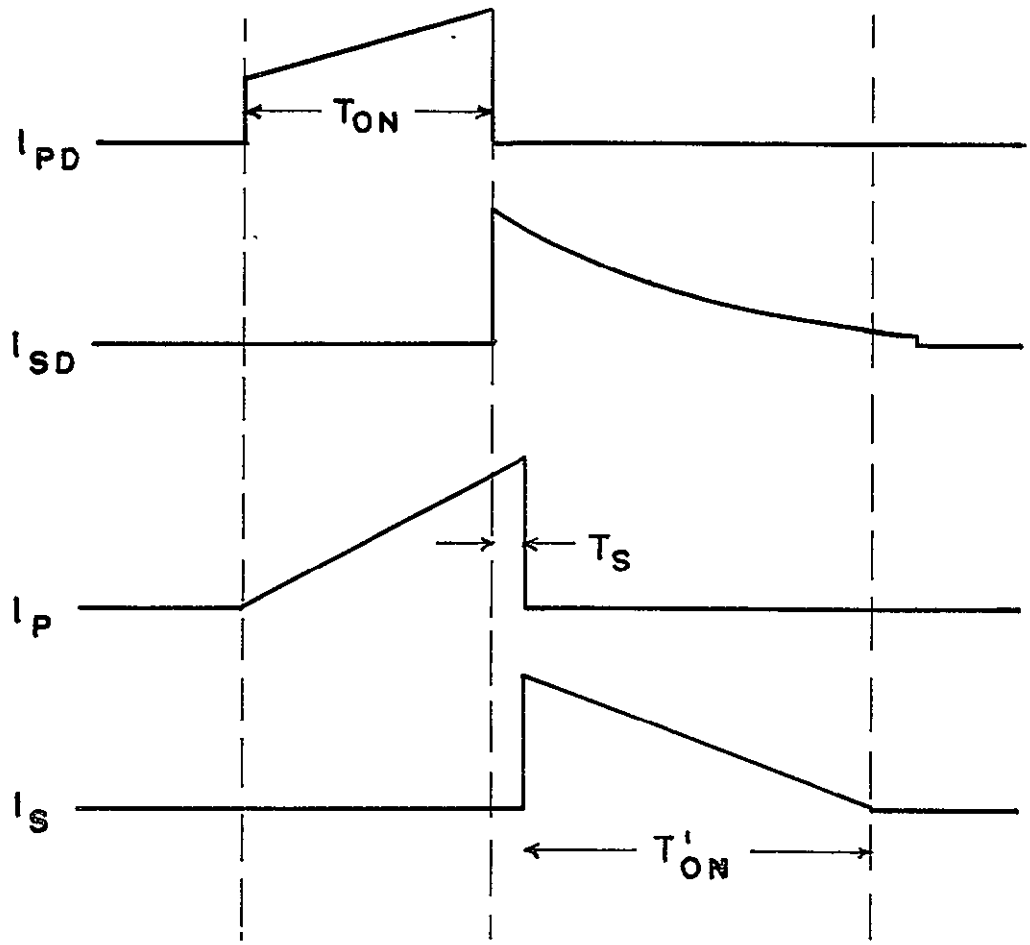


Figure 3-8 (b). Current waveforms associated with T1 and T2.

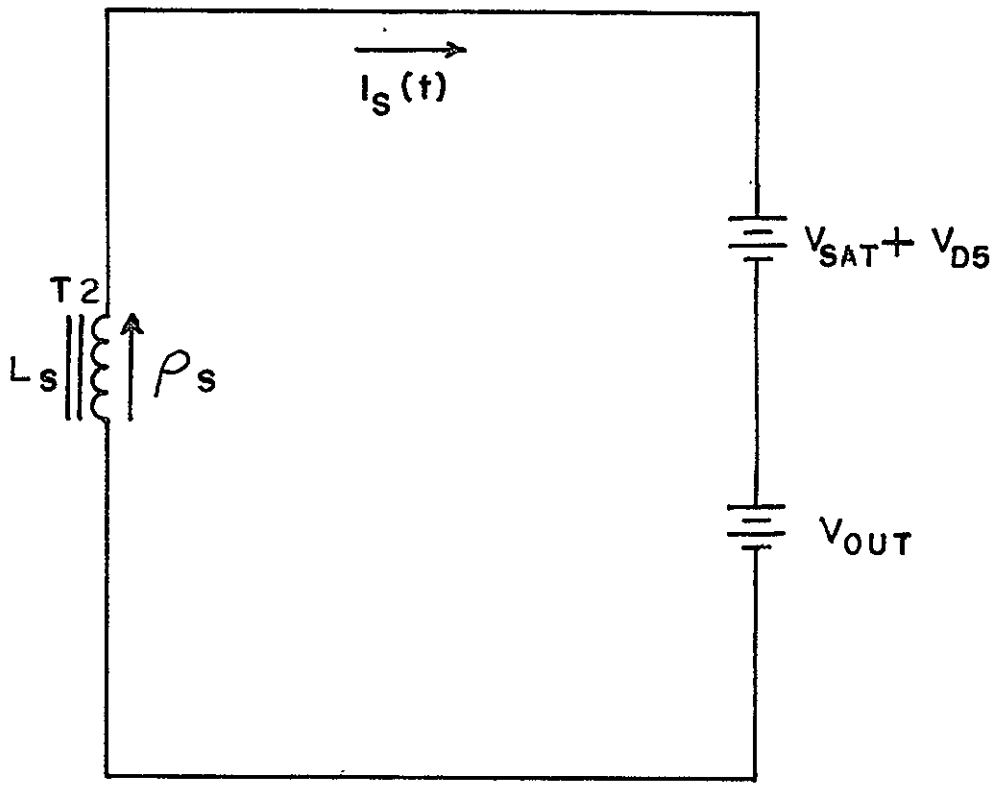


Figure 3-9. Model of output stage when Q6 is "off".

$$L_S \frac{dI_S}{dt} + V_{SAT} + V_{D5} + V_{OUT} = 0 \tag{3.5}$$

with initial condition, $I_S(0) = \rho_S$, where V_{SAT} is the saturation voltage of Q7, and V_{D5} is the forward drop across D5. Assuming the quantity $V_{SAT} + V_{D5}$ is negligible and taking the Laplace transform yields:

$$sL_S I_S(s) - L_S \rho_S = - \frac{V_{OUT}}{s} \tag{3.6}$$

$$I_S(s) = \frac{\rho_S}{s} - \frac{V_{OUT}}{s^2 L_S}$$

Therefore,

$$I_S(t) = \rho_S - \frac{V_{OUT}}{L_S} t \tag{3.7}$$

Equation (3.7) shows that the secondary current is also a ramp. Transistor Q7 gates this current to the load and, therefore, must remain "on" for a time, T'_{ON}, to allow I_S to go to zero. This time is given by:

$$T'_{ON} = \frac{\rho_S L_S}{V_{OUT}} \tag{3.8}$$

In a previous study [2] a relationship was established between ρ_S and V_{OUT}:

$$V_{OUT} \simeq \rho_S \frac{L_S R_L f}{2} \tag{3.9}$$

The substitution of (3.9) into (3.7) yields:

$$T'_{ON} \simeq \frac{2L_S}{R_L f} \tag{3.10}$$

where R_L is the load resistance and f is the switching frequency. Equation (3.10) shows that T'_{ON} is independent of ρ_S and (3.9) shows that the output voltage is proportional to ρ_S. Due to the unique operation of the output stage, the pulse-width-modulated signal is converted to a pulse-amplitude-modulated signal. A photograph of the output current (I_S) is shown in Figure 3-10 along with the voltage waveform (e_5) at the collector of Q6.

Precautions are taken to prevent I_S from flowing while Q6 is "on" or while the opposite channel is in operation. The voltage e_6 is connected to the output filter and is equal to the output voltage at all times. When the N-channel is operating, e_6 is a negative potential and current would flow from A to B (see Figure 3-8(a)) were it not for Q7 being "off". The control for Q7 comes from the P-channel signal and Q7 will not conduct unless the P-channel is in operation.

During the operation of the P-channel, when Q6 is "on", the secondary of T2 becomes a potential source with a positive voltage from A to B. The diode D_5 is reverse biased and prevents secondary current flow.

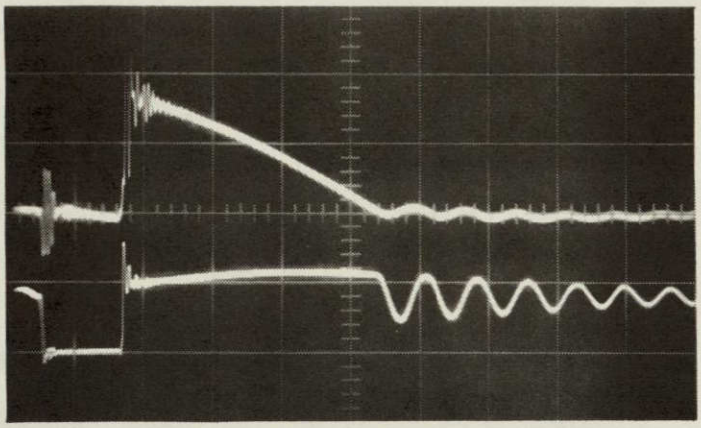


Figure 3-10. Upper trace - Output current (I_S).
Lower trace - Voltage at collector of Q6.

The output gate, Q7, must be saturated when Q6 turns "off" and remain saturated for a time, T'_{ON}, as derived above. In order to saturate Q7 before Q6 turns "off" advantage is taken of the saturation time of Q6. Figure 3-8(b) shows the saturation time, T_S, with respect to the current waveforms. The base drive circuitry is designed to saturate Q7 even at the peak value of I_S. I_S is in the form of a ramp, thus the necessary saturation base current of Q7 is also a ramp as indicated by the solid line of Figure 3-11.

The equivalent circuit of the base drive is shown in Figure 3-12. The differential equation for this circuit is:

$$L_{SD} \frac{dI_{SD}}{dt} + R7\ I_{SD} + V_{BE} = 0 \tag{3.11}$$

where $I_{SD}(0) = \rho_{SD}$ and the initial current ρ_{SD} is related to the final current in the primary, ρ_{PD}, by $\rho_{SD} = \rho_{PD} \frac{N_{PD}}{N_{SD}}$. The Laplace transform of (3.11), neglecting V_{BE} yields:

$$sL_{SD}I_{SD}(s) - \rho_{SD}L_{SD} + R7I_{SD}(s) = 0 \tag{3.12}$$

$$I_{SD}(s) = \frac{\rho_{SD}}{s + \frac{R7}{L_{SD}}}$$

so,

$$I_{SD}(t) = \rho_{SD} \exp(-\frac{R7}{L_{SD}} t) \tag{3.13}$$

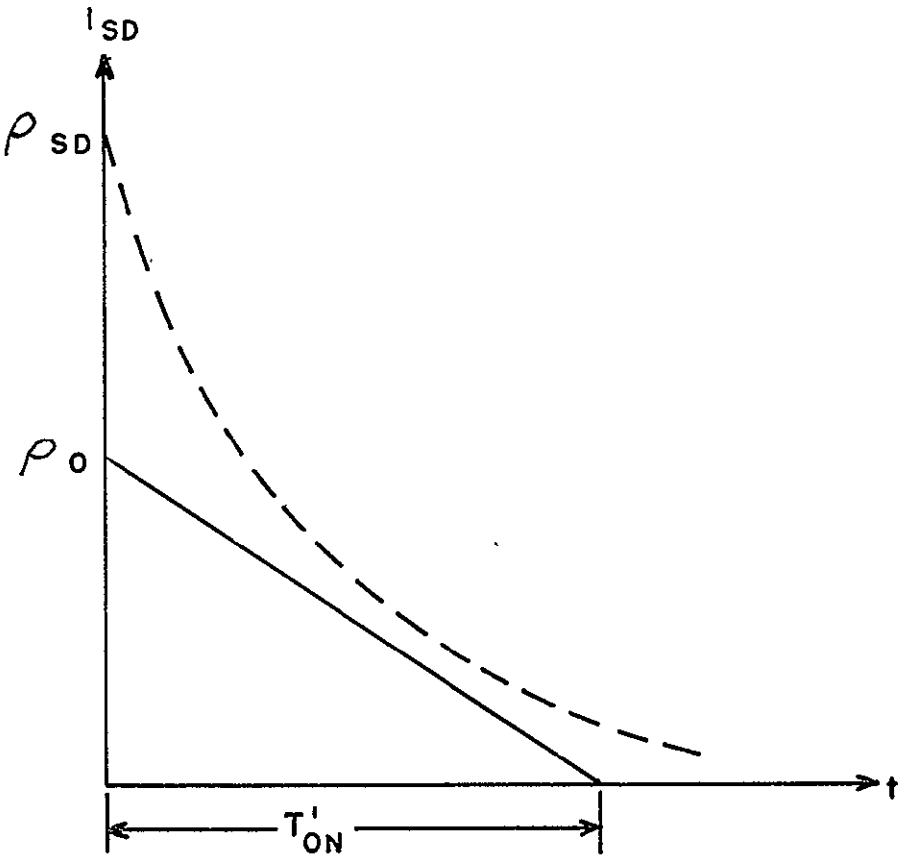


Figure 3-11. Base current of Q7.

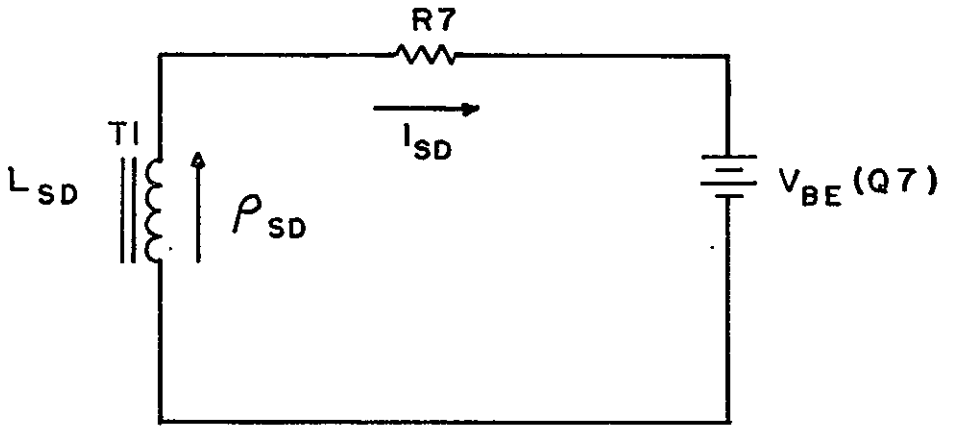


Figure 3-12. Equivalent circuit of base drive of Q7.

Equation (3.13) reveals I_{SD} to be an exponentially decaying current with a maximum value of ρ_{SD}. This current (shown by the dotted line of Figure 3-11) must at all times be above the minimum current required for saturation. The equation for the solid line of Figure 3-11 is:

$$I_O = \rho_O - \frac{\rho_O}{T'_{ON}} t, \quad 0 < t < T'_{ON} \tag{3.14}$$

and the equation for the dotted line is:

$$I_{SD} = \rho_{SD} \exp(-\frac{R7}{L_{SD}} t), \quad t > 0 \tag{3.13}$$

The only requirement to be met is:

$$I_{SD} > I_O, \quad 0 < t < T'_{ON}$$

or

$$\rho_{SD} \exp(-\frac{R7}{L_{SD}} t) > \rho_O - \frac{\rho_O}{T'_{ON}} t, \quad 0 < t < T'_{ON} \tag{3.15}$$

IV. OUTPUT FILTER

The output filter in this amplifier is designed to recover the input signal. As a consequence of the unique output stage of this amplifier the pulse-width-modulated signal is converted into a pulse-amplitude-modulated signal from which information can be recovered by a low-pass filter. The current entering the filter is depicted in Figure 4-1 where T'_{ON} and T are constant values. The period T is the period of the switching frequency and corresponds to a frequency of 200 kHz. The problem is to design a filter to attenuate the carrier and inter-modulation sideband frequencies such that a low amount of spurious frequencies are present at the load. A three-pole π-section filter, shown in Figure 4-2, is used with a cutoff frequency that is three octaves below 200 kHz. This places the cutoff frequency at f_n = 25 kHz and at a fall-off rate of 6 dB/octave-pole. The 3-pole filter attenuates the carrier by:

$$\frac{6 \text{ dB}}{\text{octave-pole}} \text{ (3 poles) (3 octaves)} = 54 \text{ dB} \qquad (4.1)$$

The next problem to be considered is the placement of the poles. The maximally-flat criteria is used which places the poles 60° apart as shown in Figure 4-3. This criteria was selected because it allows for a flat response from very low frequencies to very high frequencies with a standard roll-off and is 3-dB down at the cutoff frequencies.

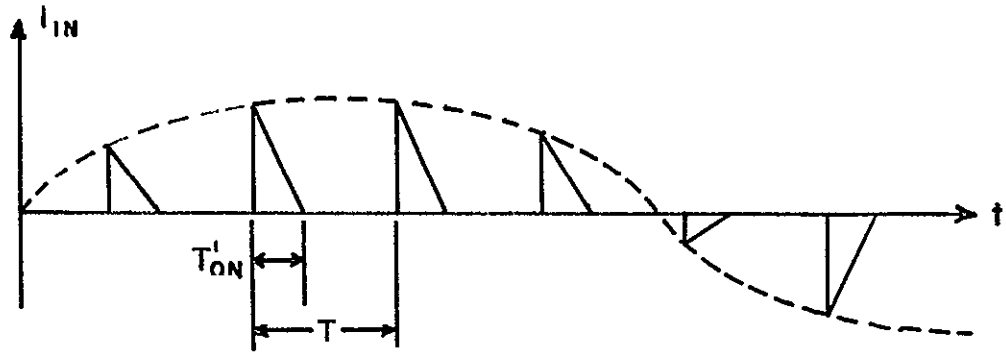


Figure 4-1. Unfiltered output current.

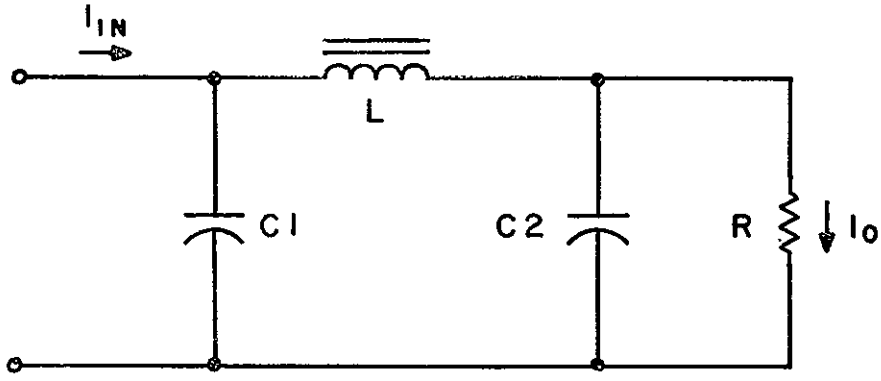
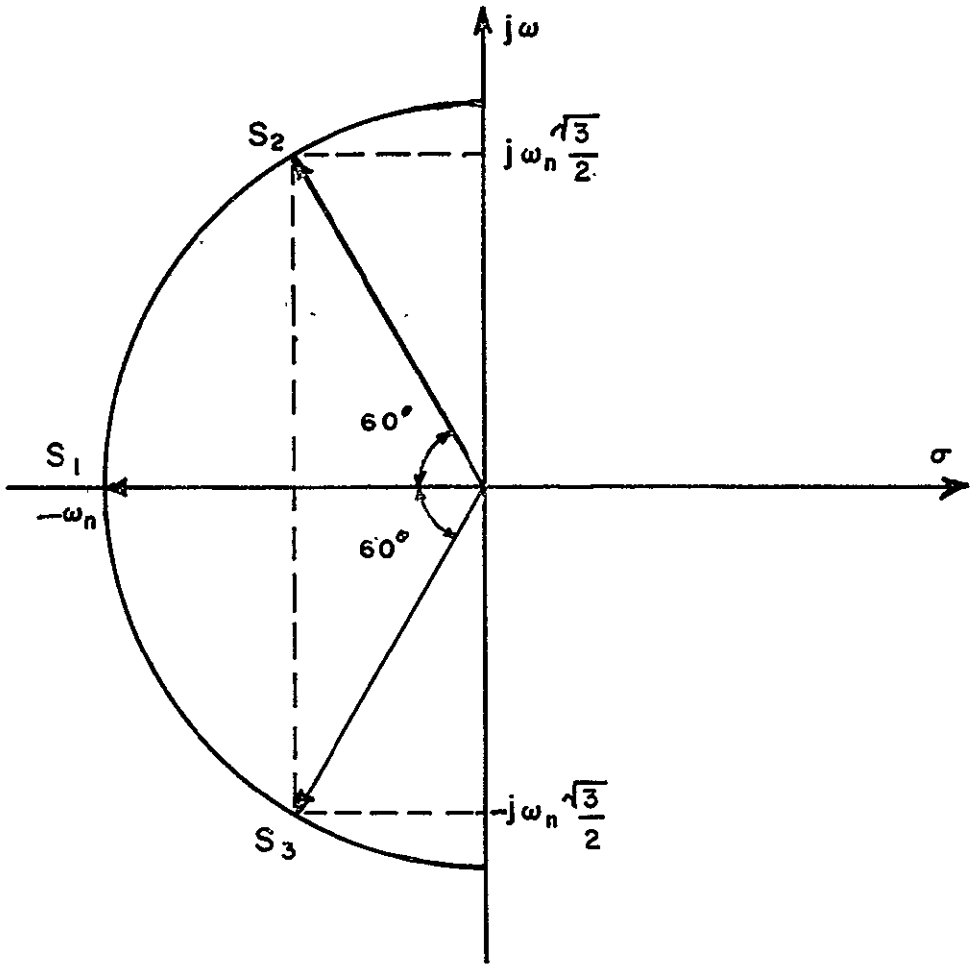


Figure 4-2. Schematic of output filter.



$$S - S_1 = S + \omega_n$$

$$S - S_2 = S + \left(\frac{1}{2} + j\frac{\sqrt{3}}{2}\right)\omega_n$$

$$S - S_3 = S + \left(\frac{1}{2} - j\frac{\sqrt{3}}{2}\right)\omega_n$$

Figure 4-3. Pole locations of maximally-flat filter.

All of these characteristics are desirable for this application.

The filter has the following transfer function:

$$\frac{I_0}{I_{IN}} = \frac{\frac{1}{C_1C_2LR}}{s^3 + s^2\frac{1}{C_2R} + s\frac{C_1 + C_2}{LC_1C_2} + \frac{1}{C_1C_2LR}} \tag{4.2}$$

From the pole locations the response of the system is desired to be;

$$\frac{I_0}{I_{IN}} = \frac{k}{(s - s_1)(s - s_2)(s - s_3)} \tag{4.3}$$

The poles, as indicated on Figure 4-3, are substituted into equation (4.3) giving the response in terms of the desired cutoff frequency:

$$\frac{I_0}{I_{IN}} = \frac{\frac{1}{\omega^3_n}}{s^3 + 2\omega_n s^2 + 2\omega^2_n s + \omega^3_n} \tag{4.4}$$

When the coefficients of s in (4.3) and (4.4) are equated, a system of equations in terms of the cutoff frequency (ω_n) and the filter components are obtained. The system of equations is solved as follows:

$$2\omega_n = \frac{1}{RC_2} \tag{4.5}$$

$$2\omega^2_n = \frac{C_1 + C_2}{LC_1C_2} \tag{4.6}$$

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$$\omega^3_n = \frac{1}{RLC_1C_2} \tag{4.7}$$

The load, R, is normally specified by the requirements of the amplifier. A value of 70 ohms was arbitrarily selected simply to illustrate design procedure. Eq. (4.5) gives:

$$C_2 = \frac{1}{2R\omega_n} = 44.5 \text{ nF}$$

Solving (4.6) and (4.7) for LC_1C_2 yields:

$$LC_1C_2 = \frac{C_1 + C_2}{2\omega^2_n} \tag{4.6}$$

$$LC_1C_2 = \frac{1}{R\omega^3_n} \tag{4.7}$$

Therefore:

$$\frac{C_1 + C_2}{2\omega^2_n} = \frac{1}{R\omega^3_n} \tag{4.8}$$

$$C_1 = \frac{2}{R\omega_n} - C_2$$

but $C_2 = \frac{1}{2R\omega_n}$ so:

$$C_1 = 4C_2 - C_2 = 3C_2$$

$$C_1 = 134 \text{ nF}$$

Solve (4.7) for L:

$$L = \frac{1}{R\omega_n^3 C_1 C_2} = 0.6 \text{ mHy} \qquad (4.7)$$

The inductor, L, was wound on an Indiana General Ferramic toriod core, CF-108, Q-1 material which has a magnetic path length of 3.23 cm. This toroid requires 100 turns to produce 0.6 mH and will have a maximum current of :

$$I_M = \frac{V_M}{R} = \frac{14.1 \text{ V}}{70 \ \Omega} = 200 \text{ mA}$$

where V_M is determined by signal output power requirements and actually represents the maximum value of the sine wave output. The ampere-turns/meter for this inductor converted to oersteds is:

$$H = \frac{(0.2A)(10^2 t)}{3.23 \times 10^{-2} m} \frac{1 \text{ oersted}}{80 \text{ At/m}} = 7.8 \text{ oersteds}$$

According to the magnetization curve furnished with the toroid core 7.8 oersteds does not exceed the linear portion of the curve and therefore is quite acceptable.

V. TESTS AND PERFORMANCE

An experimental model of that portion of the pulse-width-modulated amplifier shown in Figure 1-3 was constructed and tested with the aid of an external PWM modulator. This modulator provides both a P-channel and an N-channel PWM signal which are fed directly into the crossover detectors.

Figure 5-1 shows the results of the dc linearity tests for both channels. The output voltage is plotted as a function of the pulse width.

Figure 5-2 shows the dc efficiency of each channel plotted as a function of the output voltage. Both channels operate approximately 80% efficiency at peak voltage levels. The ac efficiency test results are shown in Figure 5-3.

Figure 5-4(a) shows the input and output waveforms at a frequency of 1 kHz and Figure 5-4(b) shows the input and output signals at 10 kHz. Both of these output waveforms were obtained with the amplifier operating in the open-loop mode. The reduction in distortion through the use of negative feedback was demonstrated by placing a feedback network from the output of the amplifier to the modulator. Figure 5-5 illustrates the results of the previous test when repeated in the closed-loop mode. Figure 5-5(a) shows the 1 kHz signals and Figure 5-5(b) shows the 10 kHz signals. The use of negative feedback produces a noticeable improvement in the 1 kHz signal but distorts the 10 kHz signal slightly. This is

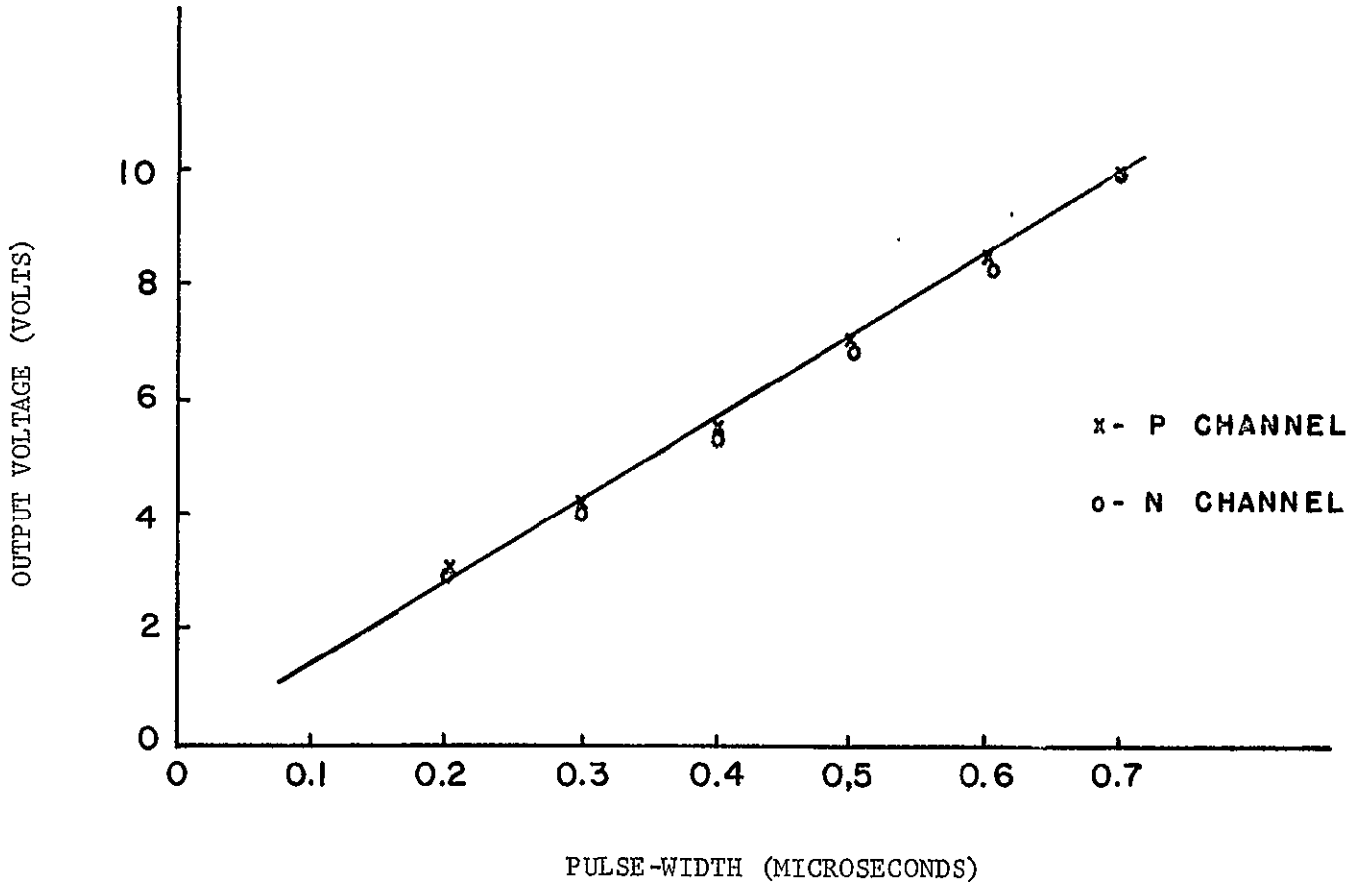

Figure 5-1. Output voltage versus pulse width.

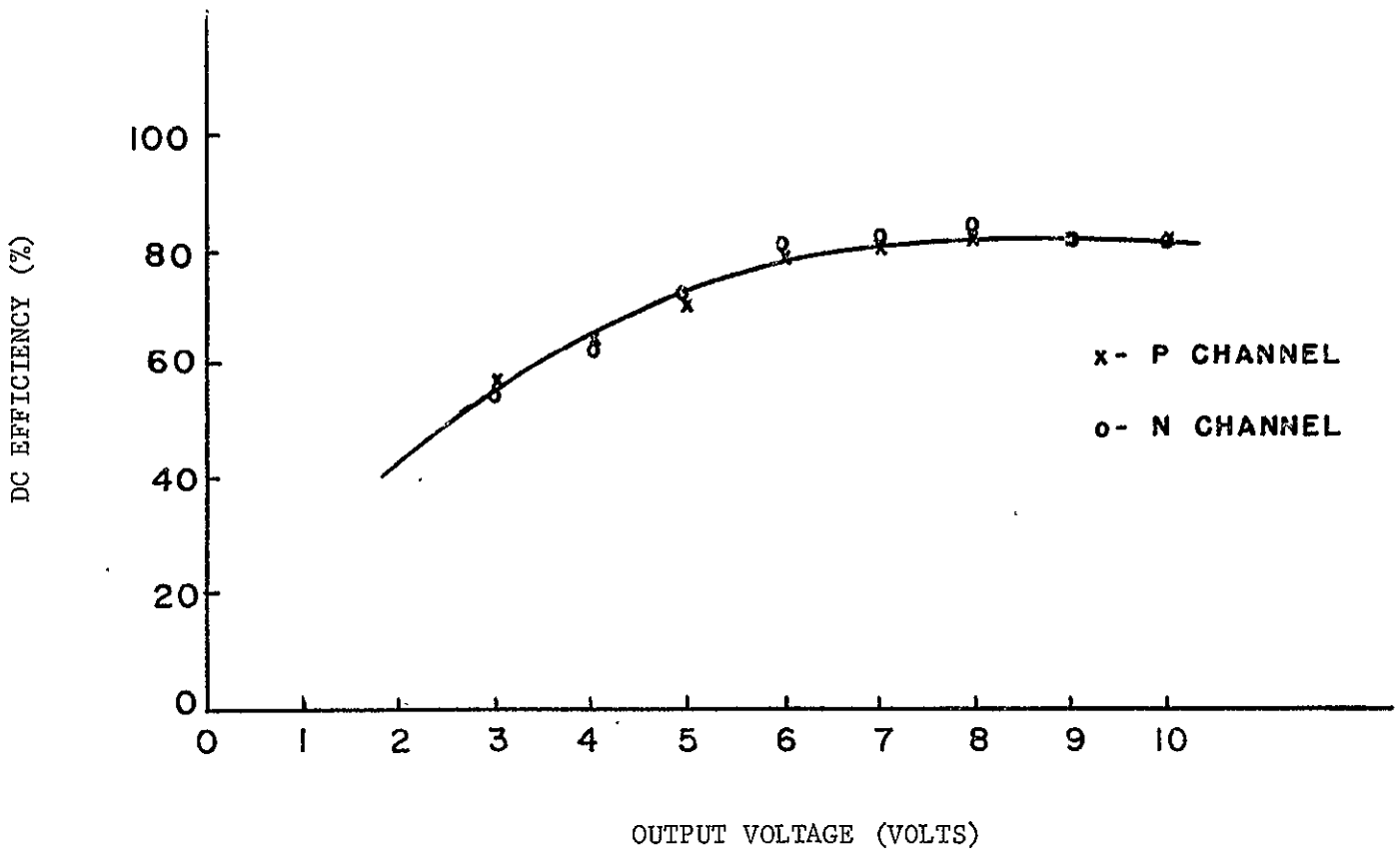

Figure 5-2. The dc efficiency of the P and N channels.

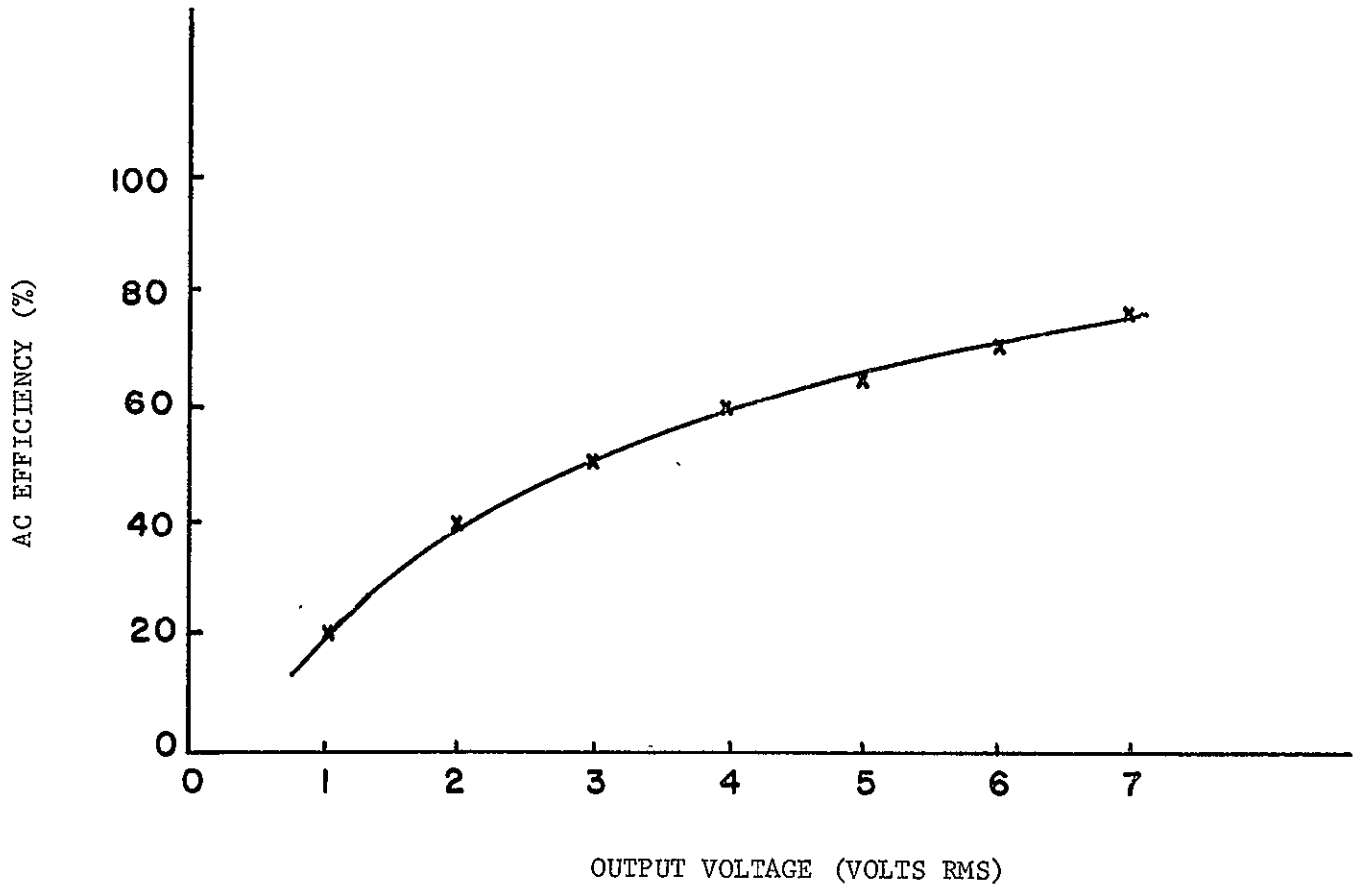

Figure 5-3. Ac efficiency test.

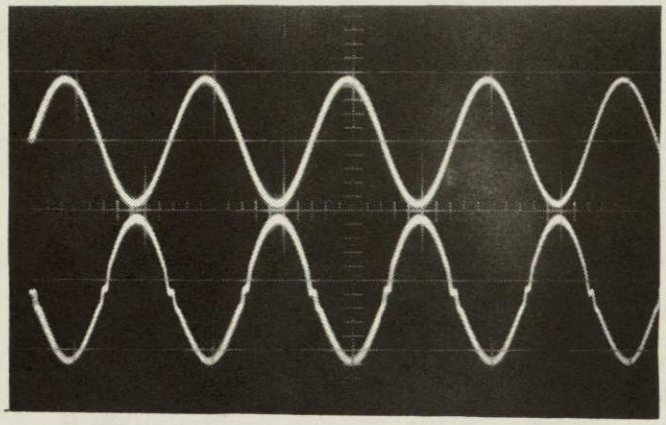

Figure 5-4 (a). Input (top) and output (bottom) at 1 kHz--open loop.

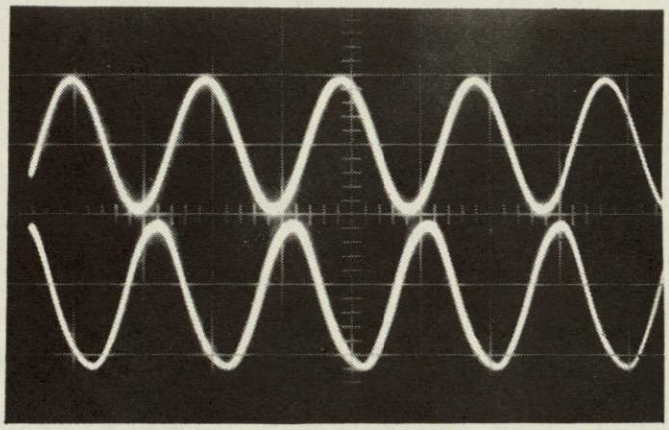

Figure 5-4 (b). Input (top) and output (bottom) at 10 kHz--open loop.

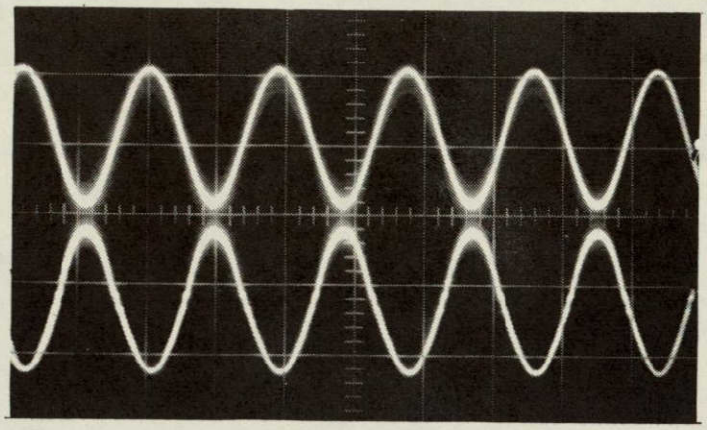

Figure 5-5 (a). Input (top) and output (bottom) at 1 kHz--closed loop.

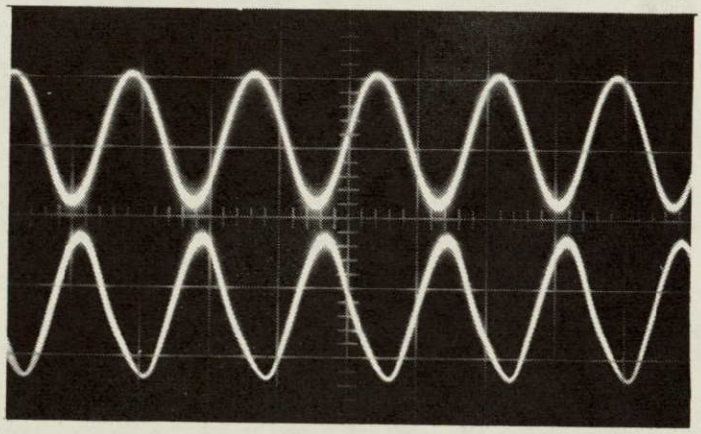

Figure 5-5 (b). Input (top) and output (bottom) at 10 kHz--closed loop.

believed to be caused by the fact that, although the gain of the amplifier is 3 dB down at 30 kHz at the filter output, the phase shift causes the third harmonic of the 10 kHz signal to be almost in phase with the input signal. However, the feedback network employed here was a pure resistive network and this problem could be alleviated by using a compensating feedback network.

Figure 5-6 shows the open-loop Bode plot of the overall PWM amplifier. The frequency response is flat within 0.5 dB from dc to 20 kHz with an overall gain of 20 dB. The graph only shows the response from 100 Hz to 20 kHz in order to give more detail to the roll-off characteristics. The input amplifier, in the modulator unit, has a variable gain and 20 dB was arbitrarily chosen for illustration. This particular gain setting gives the amplifier a 16 dB gain margin. The feedback network would, therefore, have to have a gain of -16 dB or less at this frequency or the amplifier will oscillate.

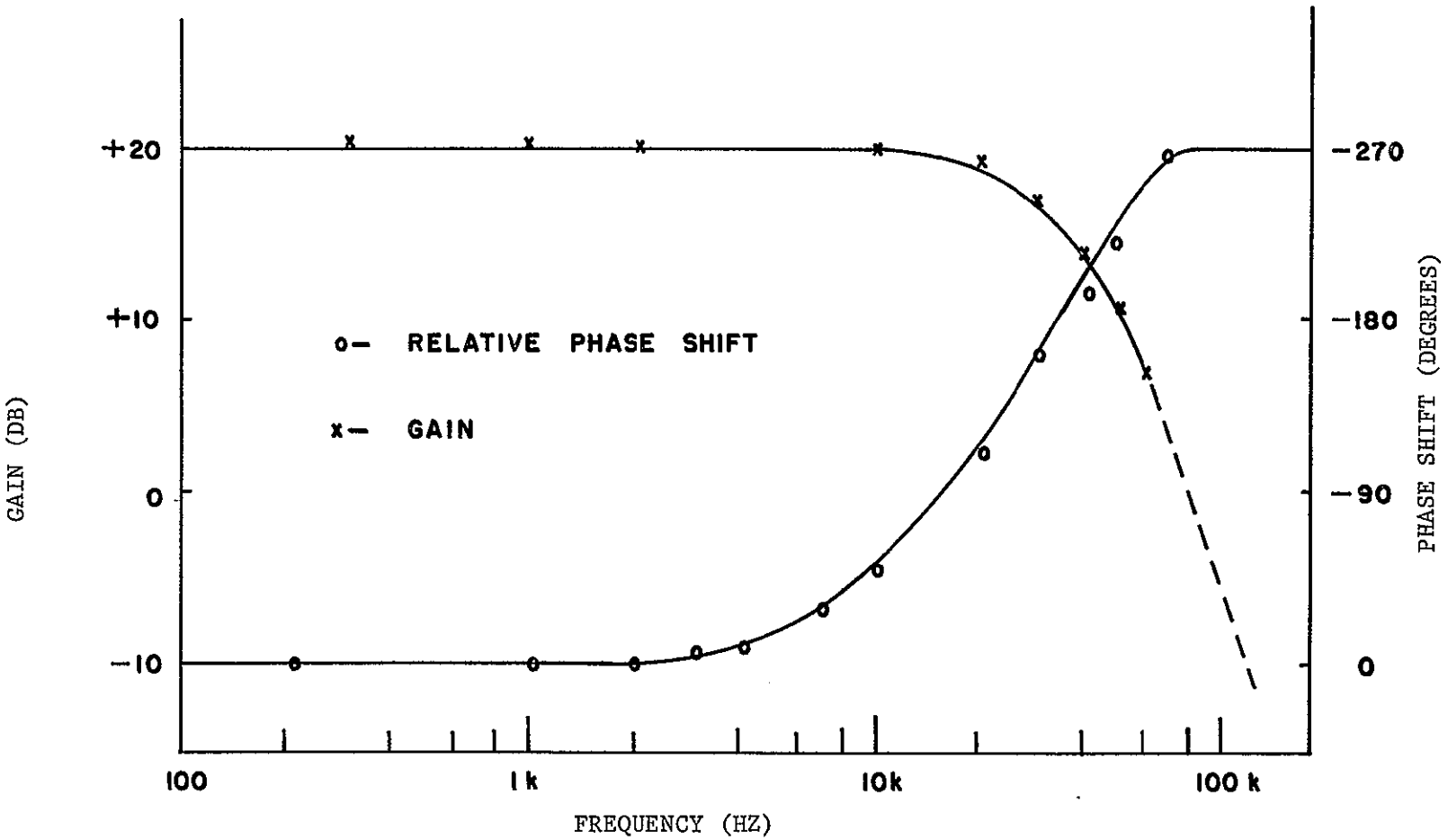

Figure 5-6. Open-loop Bode plot.

VI. CONCLUSIONS

The primary objective of this study, to develop a PWM amplifier with a frequency response from dc to 20 kHz was satisfactorily achieved. The secondary objective of a reduction in size was facilitated by increasing the switching-frequency to 200 kHz. This decreases the maximum width of the information pulse to one microsecond, which presents the problem of finding a power transistor that can switch high currents fast enough that the combined turn-on and turn-off times are small compared to one microsecond. The power amplifier used in this design switches peak currents of 0.7 amperes in a combined turn-on and turn-off time of 30 nanoseconds. The output waveform will be considerably distorted unless very fast diodes are used for the output (D5 and D10).

The transformers must be tightly wound and the leads kept as short as possible in order to minimize the leakage inductance.

REFERENCES

1. M. A. Honnell et. al., Design and Construction of a Pulse-Width-Modulated Signal Generator, Engineering Experiment Station, Auburn University, Auburn, Alabama, March, 1970.

2. M. A. Honnell et. al; An 800 Hz Switching-Mode Amplifier, Engineering Experiment Station, Auburn University, Auburn, Alabama, July, 1969.

3. David J. Comer, Introduction to Semiconductor Circuit Design, Reading, Massachusetts: Addison Wesley, 1968, pp. 251-253.

APPENDIX A

OUTPUT TRANSFORMER

The output stage of this amplifier uses a transformer in order to provide dc isolation from the load. This produces two problems; (1) The bulk of a transformer is an undesirable addition to the physical size of the amplifier; (2) there are always a certain amount of core losses to consider, plus the fact that small cores are easily saturated. If the transformer is driven to saturation the signal will be distorted.

Both of these problems have a common solution. If an air gap is formed in the toroidal core the total permeability is lowered considerably. As a result, the same inductance on the gapped core requires a much higher current to achieve saturation. This resolves the first problem since a smaller toroid can be used and the air gap prevents it from saturating under the high output currents. The use of an air gap also reduces the core losses since most of the energy is stored in the air gap which has no residual magnetism. The energy stored in the magnetic field is given by:

$$W_M = \frac{1}{2} LI^2 \text{ joules}$$

$$W_M = \frac{1}{2} \frac{N^2 A}{\frac{\ell}{\mu} + \frac{d}{\mu_o}} \left[\frac{B}{N} \left(\frac{\ell}{\mu} + \frac{d}{\mu_o}\right)\right]^2 \text{ joules}$$

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$$W_M = \frac{1}{2} AB^2 \left(\frac{\ell}{\mu} + \frac{d}{\mu_o}\right) \text{ joules}$$

where A = cross-sectional area

B = flux density

ℓ = mag path length of toroid

d = mag path length of air gap

μ = permeability of toroid

μ_o = permeability of air.

The energy stored in the toroid is

$$W_{M1} = \frac{1}{2} AB^2 \frac{\ell}{\mu} \text{ joules}$$

where ℓ = 2.97 cm

$\mu = 6 \times 10^3 \mu_o$

so

$$W_{MI} = 2.48 \times 10^{-6} \frac{AB^2}{\mu_o} \text{ joules}$$

The energy stored in the air gap is:

$$W_{M2} = \frac{1}{2} AB^2 \frac{d}{\mu_o} \text{ joules}$$

where d = 0.254 cm

so

$$W_{M2} = 1.27 \times 10^{-3} \frac{AB^2}{\mu_o} \text{ joules}$$

The following experiment illustrates the reduction in core losses (area inside the hysteresis loop) by using a gapped core. It also shows that the gapped core requires more energy to saturate.

The experimental set-up is shown in Figure A-1. The core-wound inductor is excited by the voltage e and the horizontal input to the oscilloscope is proportional to the current I. If the resistor, R2, is made small then:

$$e \simeq e_L$$

and by selecting R1 and C such that their time constant is large with respect to the period of the input voltage then the vertical input to the oscilloscope will be proportional to $\int edt$. the magnetic field intensity (H) is proportional to I and the flux density (B) is proportional to $\int edt$ and therefore the oscilloscope trace is proportional to the actual hysteresis loop (B-VS-H).

The toroid core used in this experiment is the same as the one used in the amplifier and it is an Indiana General CF-108, 06. This toroid, with an arbitrary number of turns on it, was driven into saturation and the current (I_M) was measured. The inductance (L_M) was measured and the energy supplied was calculated by:

$$W_M = \frac{1}{2} L_M I^2_M$$

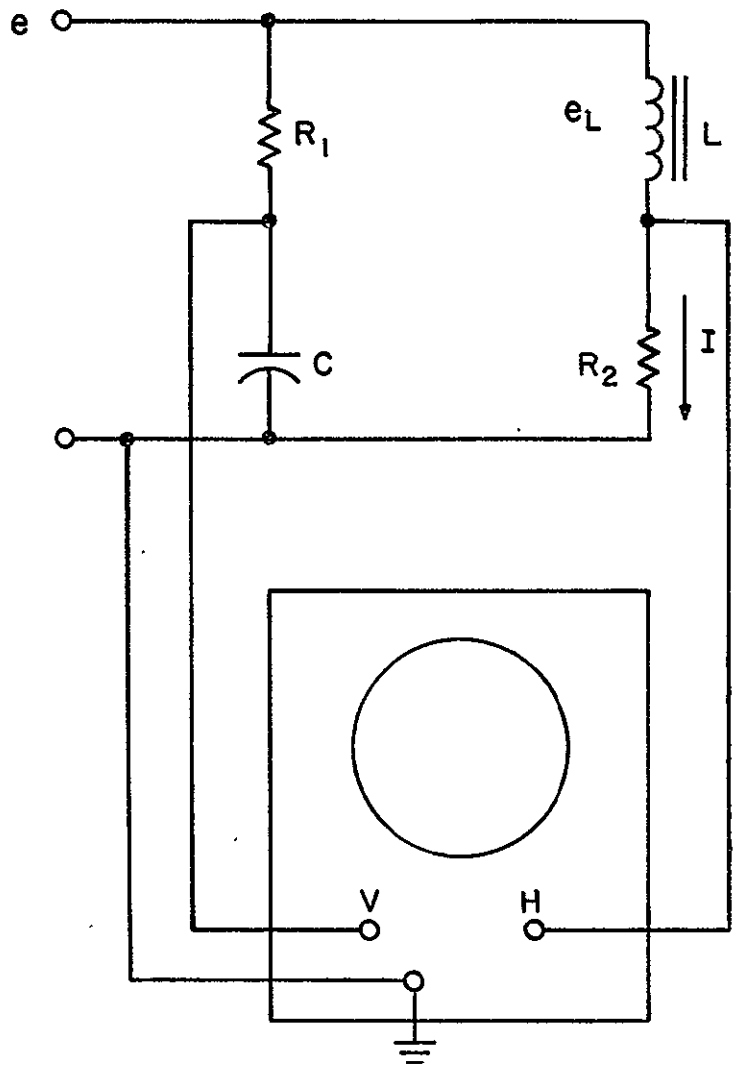

Figure A-1. Hysteresis loop experiment.

and recorded. An oscilloscope photograph of the resulting hysteresis loop is shown in Figure A-2. The same toroid was provided with an air gap of d = 0.1 in. and an arbitrary number of turns. The inductance was then measured and it was determined how much current was necessary to supply this inductor with the same energy as that of the ungapped core. The inductor was driven with this amount of current and the resulting hysteresis loop is shown in Figure A-3. Comparison of the two hysteresis loops shows the reduction of core losses and the gapped core is obviously not saturated.

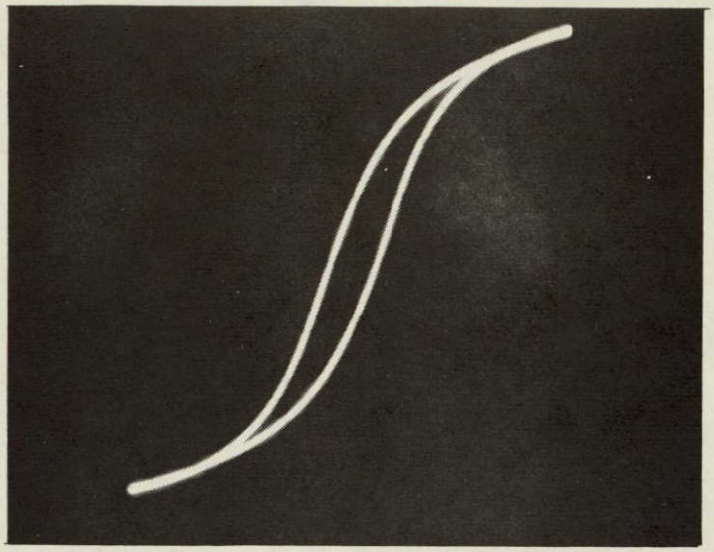

Figure A-2. Hysteresis loop of core without air gap.

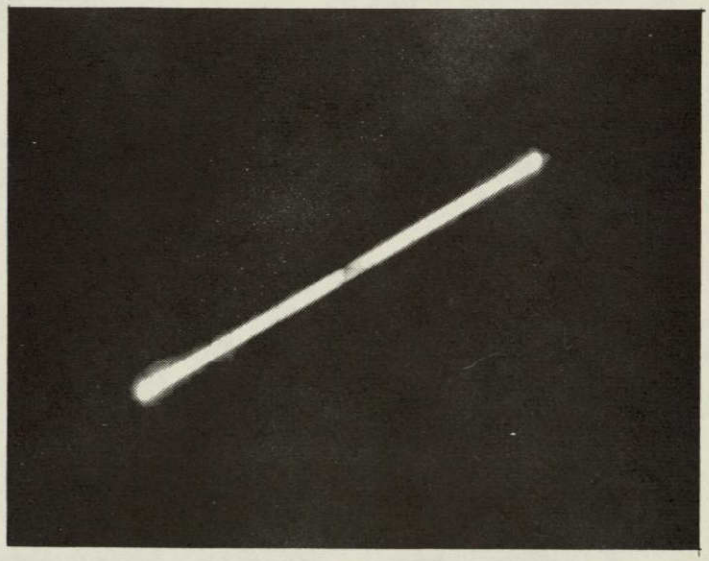

Figure A-3. Hysteresis loop of core with air gap.

APPENIDX B

DESIGN EXAMPLE

It is desired to design a switching-mode amplifier with the specifications shown in Table 1.

TABLE 1

Must use transformer output for dc isolation purposes.	
Output voltage	7 volts rms
Load	70 ohms
Frequency	dc to 20 kHz
Carrier attenuation	50 dB
Power supplies required	+28 V
	$\pm$5 V

The first consideration must be the switching frequency. The amplifier must have a frequency response up to 20 kHz. The output filter used in this example is a three-pole π-section filter (see Chapter IV). The cutoff frequency of the filter is 25 kHz and attenuates the higher frequencies at a rate of 18 dB/octave. If the carrier were three octaves above 25 kHz (200 kHz) it would be attenuated 54 dB by this filter. This 4 dB margin was assumed and the carrier was selected to be 200 kHz.

This design example is concerned only with the driver and output stage as presented in Chapter III.

The desired output voltage is 7 volts rms into a load of 70 ohms. This requires the amplifier to produce a peak power of approximately 1.5 watts. Assuming an 80% efficiency raises the peak power at the primary of the output transformer to approximately 2.0 watts.

The energy per cycle is given by:

$$P = Ef$$

$$E = \frac{2.0 \text{ watts}}{2.0 \times 10^5 \text{ Hz}} = 1 \times 10^{-5} \text{ joules}$$

The peak primary current and the inductance is now determined from the two equations:

$$E = \frac{1}{2} \rho_P^2 L_P = 10^{-5} \text{ joules}$$

and

$$\rho_P = \frac{28}{L_P} t$$

Selecting t to be 1.0 microsecond, for a reasonable duty cycle, T_{ON}, gives:

$$\frac{1}{2}\rho^2{}_P L_P = 10^{-5} \text{ joules}$$

$$\rho_P = \frac{28}{L_P} \times 10^{-6}$$

Solving these equations for ρ_P and L_P gives:

$$\rho_P = 0.7 \text{ A}$$

$$L_P = 40 \text{ } \mu\text{Hy}$$

Similarly, the secondary current is determined:

$$P = \frac{V^2_{OUT}}{RL} = E(f)(0.8)$$

where 0.8 is the efficiency, $E = 10^{-5}$ joules, and f = 200 kHz. Solving for V_{OUT} gives

$$V_{OUT} = 10.6 \text{ V}$$

Knowing the output voltage and allowing 2.5 microseconds for the discharge time gives:

$$E = \frac{1}{2}\rho^2{}_S L_S = 10^{-5} \text{ joules}$$

$$\rho_S = \frac{V_{OUT}}{L_S} t = \frac{10.6\ V}{L_S} (2.5 \times 10^{-6}\ sec)$$

Solving these equations for ρ_S and L_S gives:

$$\rho_S = 0.7\ A$$

$$L_S = 40\ \mu Hy$$

The selection of the core for the output transformer T2 is presented in Appendix A. The core with a $\frac{1}{10}$" air gap required 30 turns to produce 40 μHy. This number was determined experimentally.

The output transistor and gate transistor must carry a peak current of 700 mA and, because of the high switching-frequency, must be extremely fast. A 2N3507 was selected for this application. A beta of 40 is assured. With a peak collector current of 700 mA, 20 mA of base drive should prove sufficient for saturation of Q6. An I_S of 35 mA (see Figure 3-3) is used.

The base drive for Q7 (see Figure 3-11) must maintain saturation for a time T'_{ON}. ρ_O was found to be 20 mA and ρ_{SD} was selected to be 50 mA. The relationship between L_{SD} and L_{PD} is:

$$\rho^2_{SD} L_{SD} = {}^2_{PD} L_{PD}$$

$$\rho_{PD} = \frac{5V - (V_{SAT} + V_{BE})}{L_{PD}} T_{ON}$$

where V_{SAT} = saturation voltage of Q4

V_{BE} = base-emitter voltage of Q6

T_{ON} = 1 μsec

and $(V_{SAT} + V_{BE}) \simeq 1.0$ V, therefore:

$$\rho_{PD} = \frac{4}{L_{PD}} \times 10^{-6}$$

$$\rho^2_{PD} = \frac{1.6}{L^2_{PD}} \times 10^{-11}$$

and

$$\rho^2_{PD} = \frac{L_{SD}}{L_{PD}} \rho^2_{SD} = \frac{1.6}{L^2_{PD}} \times 10^{-11}$$

$$L_{PD} = \frac{1.6 \times 10^{-11}}{L_{SD} \rho^2_{SD}}$$

but $\rho_{SD} = 50$ mA, so

$$L_{PD} = \frac{64 \times 10^{-10}}{L_{SD}}$$

Equation (3.15) states that the dotted line of Figure 3-11 must be greater than the solid line for all t, $0 < t < T'_{ON}$

$$\rho_{SD} \exp\left(-\frac{R7}{L_{SD}} t\right) > \rho_0 - \frac{\rho_0}{T'_{ON}} t \qquad (3.15)$$

At t = 0, eq. (3.15) gives:

$$\rho_{SD} > \rho_o$$

and the inequality is satisfied since ρ_{SD} = 50 mA and ρ_o = 20 mA.

At t = 1.25μ sec, eq. (3.15) gives:

$$\exp\ (-1.25\ \frac{R7}{L_{SD}} \times 10^{-6}) > 0.2 \qquad (3.15)$$

To minimize losses in the cirucit R7 should be small and was selected to be R7 = 10 ohms. Substitution of this into eq. (3.15) gives:

$$\exp\ (-\frac{1.25}{L_{SD}} \times 10^{-5}) > 0.2 \qquad (3.15)$$

This value was laboratory selected to be:

$$\exp\ (-\frac{1.25}{L_{SD}} \times 10^{-5}) = 0.85$$

$$L_{SD} \approx 80\ \mu Hy$$

The relationship between L_{SD} and L_{PD} gives:

$$L_{PD} = \frac{64 \times 10^{-10}}{L_{SD}} = 80\ \mu Hy$$

An Indiana General CF-102 Q1 core was chosen because of its small size (2.24 cm mag. path length). Information furnished with the core assured that 80 μHy could be obtained with 30 turns. The field intensity is calculated as follows:

$$H = \frac{1.28\ NI}{\text{mag. path in cm}} = 0.85 \text{ oersteds}$$

This represents a flux density of about 100 gauss which falls well within the linear portion of the B-H curve.

It was stated previously that I_S (see Figure 3-3) was selected to be 35 mA. The value of R6 (see Figure 3-2) is determined by the equation:

$$I_S = \frac{5 - (V_{D2} + V_{SAT} + e_4)}{R6}$$

where $I_S = 35$ mA

$$(V_{D2} + V_{SAT} + e_4) \simeq 1.5 \text{ V}$$

and

$$35 \times 10^{-3} = \frac{3.5}{R6}$$

$$R6 = 100 \text{ ohms}$$

The driver transistor Q4 must carry maximum of $I_S + \rho_{PD} = 85$ mA. Q4 has an even lower current requirement and the two transistors were selected primarily for their switching speeds. Q4 is 2N2369 and Q5 is a 2N2905. A complete parts list of the entire output section is given in Table 2.

TABLE 2

PARTS LIST OF THE OUTPUT STAGE SHOWN IN FIG. 1-3

Reference Symbol of Resistors	Resistance All $\frac{1}{4}$ W except RL
R1	330 ohms
R2	same as R1
R3	500 kilohms
R4	500 kilohms, pot.
R5	1 kilohms
R6	100 ohms
R7	10 ohms
R8	same as R1
R9	same as R1
R10	same as R3
R11	same as R4
R12	same as R5
R13	same as R6
R14	same as R7
R_L	70 ohms, 5 watts

TABLE 2 (continued)

Reference Symbol of Capacitors	Capacitance
C1	150 nF
C2	50 nF

Reference Symbol of Diodes	Type
D1	1N3064
D2	same as D1
D3	TI-8
D4	1N720
D5	UTX-215
D6	same as D1
D7	same as D1
D8	same as D3
D9	same as D4
D10	same as D5

Reference Symbol of Transistors	Type
Q1	2N3905
Q2	same as Q1
Q3	2N2369

TABLE 2 (continued)

Q4	same as Q3
Q5	2N2905
Q6	2N3507
Q7	same as Q6
Q8	same as Q1
Q9	same as Q1
Q10	same as Q3
Q11	same as Q5
Q12	same as Q3
Q13	same as Q6
Q14	same as Q6

Reference Symbols of Transformers	Type
T1	Core (Indiana General CF-102 Q1), primary 30 turns, secondary 30 turn.
T2	Core (Indiana General CF-108 0-6), primary 30 turns, secondary 30 turns.
T3	same as T1
T4	same as T2

Reference Symbol of Inductor	Inductance
L1	0.6 mHy